



H81H3-AD

Rev:V1.0

ECS
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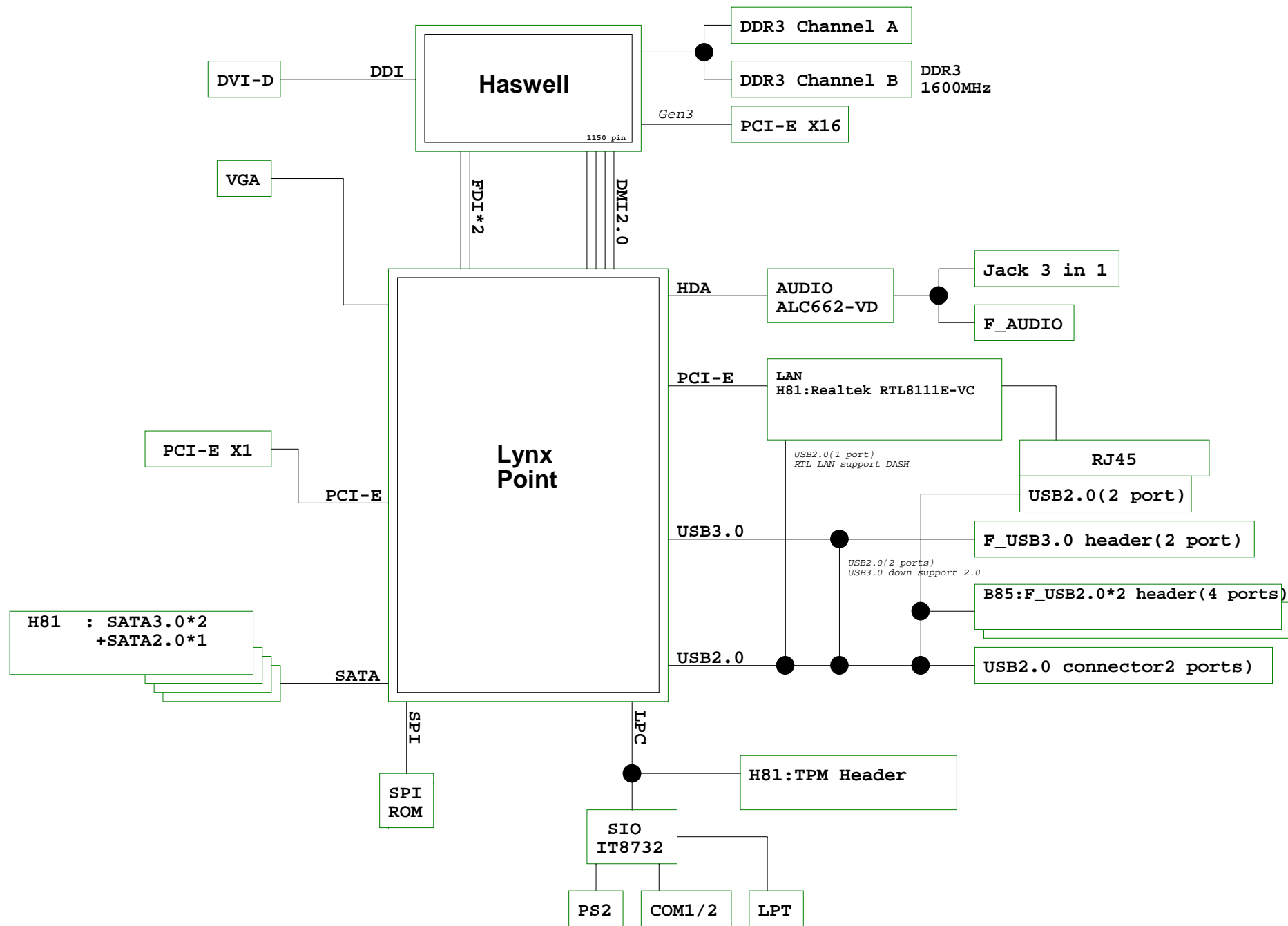
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REVISION HISTORY:

Rev	Date	Notes
A	2013/01/23	Modified Q87H3-AM to Sargo project.
B	2013/05/10	Swap BIOS_WP and CMOS header, combine bottom side of GND plane VGA and PS2.
C	2013/05/30	Cancel sparate line of Vcore in GND layer.
V1.0	2013/06/07	modified for MP.

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PCH-GPIO function

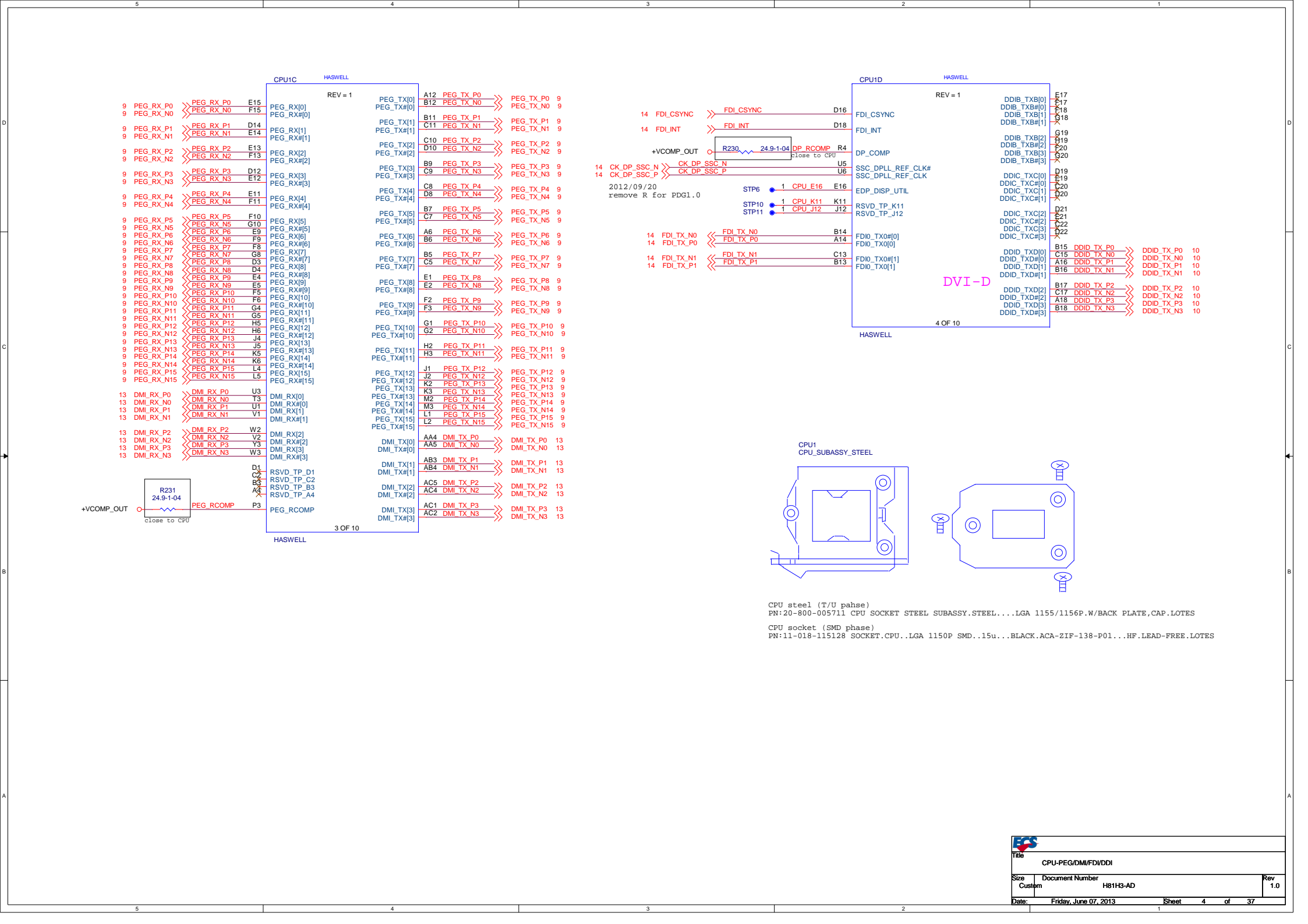
Pin Name	Power Well	Usage	Default Status	
GPIO13	3VSB	LPC_PME	GPI	
GPIO40	3VSB	USB_5VDUAL control	Native	S0/S3/S4/S5:High
GPIO72	3VSB	USB_5VDUAL control (reserve)	Native	S0/S3/S4/S5:High
GPIO45	3VSB	BIOS WP	Native	OUTPUT Low/BIOS WP, High/Normal
GPIO57	3VSB	BIOS WP	GPI	INPUT Low/Normal, High/BIOS WP
GPIO46	3VSB	WLAN_DIS_L	Native	
GPIO61	3VSB	LPCPD_L	Native	INPUT Low/Active
GPIO27	ATX_3VSB	ILAN_WAKE_L	GPI	INPUT Low/Active
GPIO1	VCC3	OBR	GPI	INPUT Low/Active
GPIO6	VCC3	Thermal_SD	GPI	INPUT Low/Active
GPIO68	VCC3	TP_VGA	GPI	INPUT Low/On VGA output
GPIO23	VCC3	HDPANEL_DETECT	Native	INPUT Low/Active
GPIO15	3VSB	PEX16_RST	GPO	S0:High S3/S4/S5:Low
DL,BIOS must be pro				
GPIO73	3VSB	case open(reserve)	PCIECLKRQ0#	
GPIO24	3VSB	ME_Disable	GPO	OUTPUT Low/Normal, High/ME disable
GPIO19	VCC3	BOOT device detect	GPI	
GPIO51	VCC3	BOOT device detect	GPO	

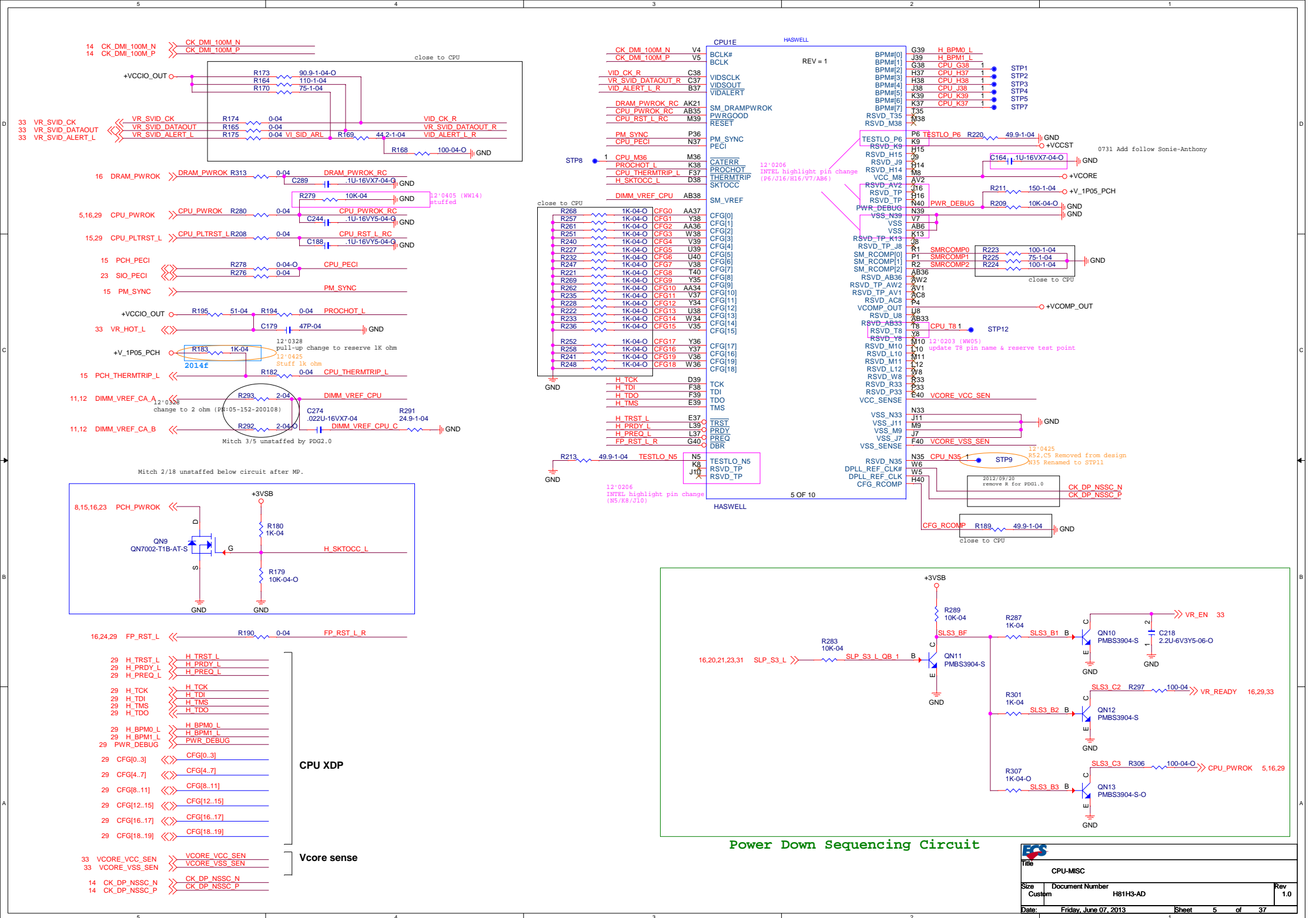
Interrupt mapping

Function	INT# port	PCle*1 port	Device
LAN	INTC#	port 3	RTL8111E-VC
PCIEX1	INTD#	port 4	LPT integrate
SATA	INTB#	NA	LPT integrate

SIO-GPIO function

Pin Name	Power Well	Usage	Default Status	
GP16	VCC3	Beep(reserve)	CIRRX2	
GP36	3VSB	Thermal_SD	FAN_CTL3	OUTPUT Low/Thermal SD, High/Normal
GP35	3VSB	LED0	FAN_TAC4	
GP37	3VSB	LED1	FAN_TAC3	
GP70	VCC3	TPM Onboard detect	GPIO	INPUT Low/TMP Header, High/TMP CHIP
GP71	VCC3	BOM detect	GPIO	
GP73	VCC3	BOM detect	GPIO	
GP74	VCC3	BOM detect	GPIO	
GP76	3VSB	Changer enable	GPIO	S0/S3/S4/S5:High
GP46	3VSB	Acer Header	GPIO	
GP47	3VSB	Acer Header	GPIO	
GP40	3VSB	5VDUAL Switch	3VSB	SW
RI1#	3VSB	LAN on MB wake up	RI1	INPUT Low/Active
BIOS must be pro to Native 3VSB				





11	M_DATA_A[0..63]	<<	M_DATA_A[0..63]
11	M_DQS_A_P[0..7]	<<	M_DQS_A_P[0..7]
11	M_DQS_A_N[0..7]	<<	M_DQS_A_N[0..7]
11	M_MA_A[0..15]	<<	M_MA_A[0..15]
11	M_BS_A[0..2]	<<	M_BS_A[0..2]
11	M_CS_A_L[0..1]	<<	M_CS_A_L[0..1]
11	M_CKE_A[0..1]	<<	M_CKE_A[0..1]
11	M_ODT_A[0..1]	<<	M_ODT_A[0..1]
11	M_CLK_A_P[0..1]	<<	M_CLK_A_P[0..1]
11	M_CLK_A_N[0..1]	<<	M_CLK_A_N[0..1]
11	M_WE_A_L	<<	M_WE_A_L
11	M_CAS_A_L	<<	M_CAS_A_L
11	M_RAS_A_L	<<	M_RAS_A_L

DDR3 CH.A

11	M_DATA_B[0..63]	<<	M_DATA_B[0..63]
11	M_DQS_B_P[0..7]	<<	M_DQS_B_P[0..7]
11	M_DQS_B_N[0..7]	<<	M_DQS_B_N[0..7]
11	M_MA_B[0..15]	<<	M_MA_B[0..15]
11	M_BS_B[0..2]	<<	M_BS_B[0..2]
11	M_CS_B_L[0..1]	<<	M_CS_B_L[0..1]
11	M_CKE_B[0..1]	<<	M_CKE_B[0..1]
11	M_ODT_B[0..1]	<<	M_ODT_B[0..1]
11	M_CLK_B_P[0..1]	<<	M_CLK_B_P[0..1]
11	M_CLK_B_N[0..1]	<<	M_CLK_B_N[0..1]
11	M_WE_B_L	<<	M_WE_B_L
11	M_CAS_B_L	<<	M_CAS_B_L
11	M_RAS_B_L	<<	M_RAS_B_L

DDR3 CH.B

6,11 DDR3_DRAMRST_L << DDR3_DRAMRST_L

**Attention

CPU1A				HASWELL			
REV = 1							
M_DATA_A0	AD38	SA_DQ[0]	SA_MA[0]	AU13 M_MA_A0			
M_DATA_A1	AD39	SA_DQ[1]	SA_MA[1]	AU16 M_MA_A1			
M_DATA_A2	AF38	SA_DQ[2]	SA_MA[2]	AU16 M_MA_A2			
M_DATA_A3	AF39	SA_DQ[3]	SA_MA[3]	AW17M_MA_A3			
M_DATA_A4	AD37	SA_DQ[4]	SA_MA[4]	AU17 M_MA_A4			
M_DATA_A5	AD40	SA_DQ[5]	SA_MA[5]	AW18M_MA_A5			
M_DATA_A6	AF37	SA_DQ[6]	SA_MA[6]	AV17 M_MA_A6			
M_DATA_A7	AF40	SA_DQ[7]	SA_MA[7]	AT18 M_MA_A7			
M_DATA_A8	AH40	SA_DQ[8]	SA_MA[8]	AU18 M_MA_A8			
M_DATA_A9	AH39	SA_DQ[9]	SA_MA[9]	AT19 M_MA_A9			
M_DATA_A10	AK38	SA_DQ[10]	SA_MA[10]	AW11M_MA_A10			
M_DATA_A11	AK39	SA_DQ[11]	SA_MA[11]	AV19 M_MA_A11			
M_DATA_A12	AH37	SA_DQ[12]	SA_MA[12]	AU19 M_MA_A12			
M_DATA_A13	AH38	SA_DQ[13]	SA_MA[13]	AY10 M_MA_A13			
M_DATA_A14	AK37	SA_DQ[14]	SA_MA[14]	AT20 M_MA_A14			
M_DATA_A15	AK40	SA_DQ[15]	SA_MA[15]	AU21 M_MA_A15			
M_DATA_A16	AM39	SA_ODT[0]	SA_ODT[0]	AW10M_ODT_A0			
M_DATA_A17	AM38	SA_ODT[1]	SA_ODT[1]	AW9 M_ODT_A1			
M_DATA_A18	AP38	SA_ODT[2]	SA_ODT[2]	AW8			
M_DATA_A19	AP39	SA_ODT[3]	SA_ODT[3]	AW33			
M_DATA_A20	AM37	SA_ODT[4]	SA_ODT[4]	AV33			
M_DATA_A21	AM38	SA_ODT[5]	SA_ODT[5]	AV31			
M_DATA_A22	AP37	SA_ODT[6]	SA_ODT[6]	AT33			
M_DATA_A23	AP40	SA_ODT[7]	SA_ODT[7]	AV33			
M_DATA_A24	AV37	SA_ODT[8]	SA_ODT[8]	AV31			
M_DATA_A25	AW37	SA_ODT[9]	SA_ODT[9]	AT33			
M_DATA_A26	AV35	SA_ODT[10]	SA_ODT[10]	AV33			
M_DATA_A27	AV35	SA_ODT[11]	SA_ODT[11]	AV31			
M_DATA_A28	AT37	SA_ODT[12]	SA_ODT[12]	AT33			
M_DATA_A29	AU37	SA_ODT[13]	SA_ODT[13]	AV33			
M_DATA_A30	AT35	SA_ODT[14]	SA_ODT[14]	AV31			
M_DATA_A31	AW35	SA_ODT[15]	SA_ODT[15]	AT33			
M_DATA_A32	AV36	SA_ODT[16]	SA_ODT[16]	AV31			
M_DATA_A33	AV36	SA_ODT[17]	SA_ODT[17]	AT33			
M_DATA_A34	AV4	SA_ODT[18]	SA_ODT[18]	AV31			
M_DATA_A35	AU4	SA_ODT[19]	SA_ODT[19]	AT33			
M_DATA_A36	AW6	SA_ODT[20]	SA_ODT[20]	AV31			
M_DATA_A37	AW4	SA_ODT[21]	SA_ODT[21]	AT33			
M_DATA_A38	AW4	SA_ODT[22]	SA_ODT[22]	AV31			
M_DATA_A39	AY4	SA_ODT[23]	SA_ODT[23]	AT33			
M_DATA_A40	AR1	SA_ODT[24]	SA_ODT[24]	AV31			
M_DATA_A41	AR1	SA_ODT[25]	SA_ODT[25]	AT33			
M_DATA_A42	AN3	SA_ODT[26]	SA_ODT[26]	AV31			
M_DATA_A43	AN4	SA_ODT[27]	SA_ODT[27]	AT33			
M_DATA_A44	AR2	SA_ODT[28]	SA_ODT[28]	AV31			
M_DATA_A45	AR3	SA_ODT[29]	SA_ODT[29]	AT33			
M_DATA_A46	AN2	SA_ODT[30]	SA_ODT[30]	AV31			
M_DATA_A47	AN1	SA_ODT[31]	SA_ODT[31]	AT33			
M_DATA_A48	AL1	SA_ODT[32]	SA_ODT[32]	AV31			
M_DATA_A49	AL4	SA_ODT[33]	SA_ODT[33]	AT33			
M_DATA_A50	AJ3	SA_ODT[34]	SA_ODT[34]	AV31			
M_DATA_A51	AJ4	SA_ODT[35]	SA_ODT[35]	AT33			
M_DATA_A52	AL2	SA_ODT[36]	SA_ODT[36]	AV31			
M_DATA_A53	AL3	SA_ODT[37]	SA_ODT[37]	AT33			
M_DATA_A54	AJ2	SA_ODT[38]	SA_ODT[38]	AV31			
M_DATA_A55	AJ1	SA_ODT[39]	SA_ODT[39]	AT33			
M_DATA_A56	AG1	SA_ODT[40]	SA_ODT[40]	AV31			
M_DATA_A57	AG4	SA_ODT[41]	SA_ODT[41]	AT33			
M_DATA_A58	AE3	SA_ODT[42]	SA_ODT[42]	AV31			
M_DATA_A59	AE4	SA_ODT[43]	SA_ODT[43]	AT33			
M_DATA_A60	AG2	SA_ODT[44]	SA_ODT[44]	AV31			
M_DATA_A61	AG3	SA_ODT[45]	SA_ODT[45]	AT33			
M_DATA_A62	AE2	SA_ODT[46]	SA_ODT[46]	AV31			
M_DATA_A63	AE1	SA_ODT[47]	SA_ODT[47]	AT33			
M_DQS_A_P0	AE39	SA_DQS[0]	SA_DQS[0]	AV35			
M_DQS_A_P1	AJ39	SA_DQS[1]	SA_DQS[1]	AV35			
M_DQS_A_P2	AN39	SA_DQS[2]	SA_DQS[2]	AT35			
M_DQS_A_P3	AV36	SA_DQS[3]	SA_DQS[3]	AV35			
M_DQS_A_P4	AV5	SA_DQS[4]	SA_DQS[4]	AT35			
M_DQS_A_P5	AP3	SA_DQS[5]	SA_DQS[5]	AV35			
M_DQS_A_P6	AK3	SA_DQS[6]	SA_DQS[6]	AT35			
M_DQS_A_P7	AF3	SA_DQS[7]	SA_DQS[7]	AV35			
M_DQS_A_N0	AE38	SA_DQS[8]	SA_DQS[8]	AT35			
M_DQS_A_N1	AJ38	SA_DQS[9]	SA_DQS[9]	AV35			
M_DQS_A_N2	AN38	SA_DQS[10]	SA_DQS[10]	AT35			
M_DQS_A_N3	AV36	SA_DQS[11]	SA_DQS[11]	AV35			
M_DQS_A_N4	AW5	SA_DQS[12]	SA_DQS[12]	AT35			
M_DQS_A_N5	AP2	SA_DQS[13]	SA_DQS[13]	AV35			
M_DQS_A_N6	AK2	SA_DQS[14]	SA_DQS[14]	AT35			
M_DQS_A_N7	AF2	SA_DQS[15]	SA_DQS[15]	AV35			
M_DQS_A_N8	AU32	SA_DQS[16]	SA_DQS[16]	AT35			

SA_RAS

SA_WE

RSVD_AV20

RSVD_AW27

SA_CAS

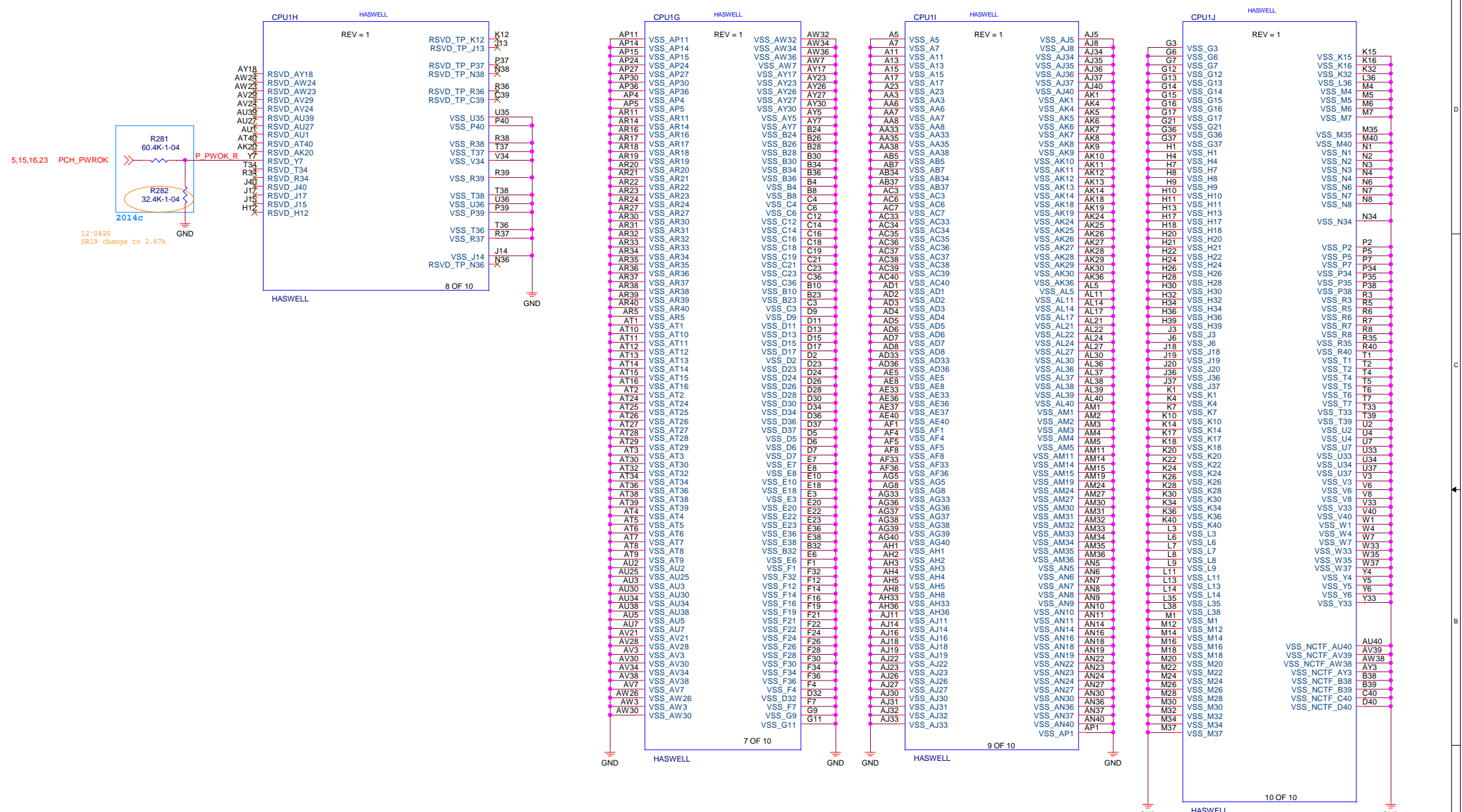
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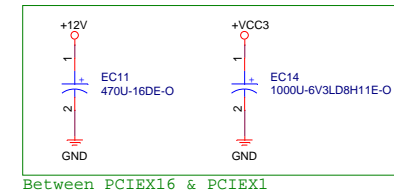
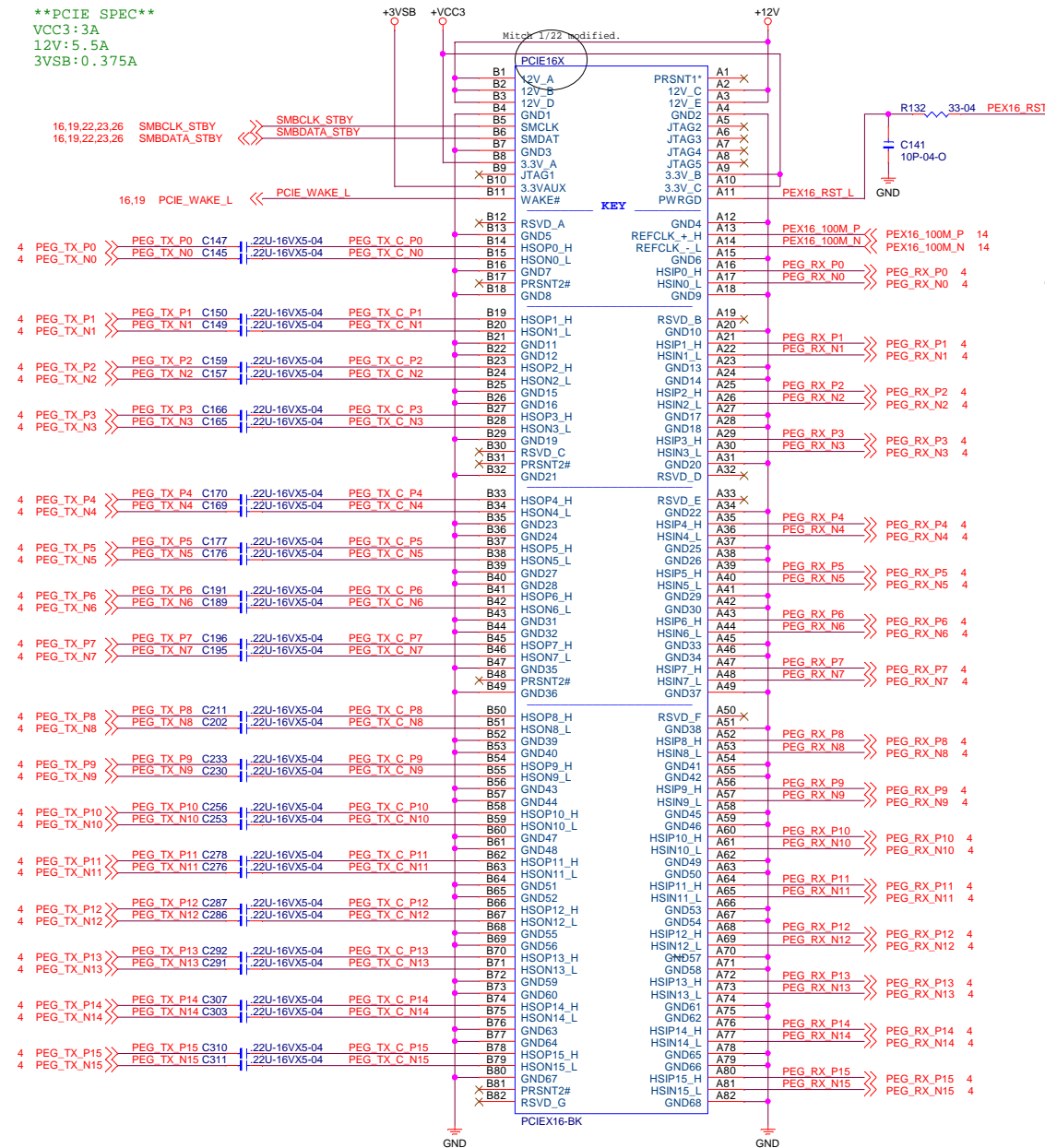
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**Attention

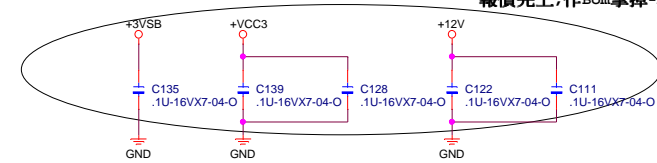
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REV = 1				
M_DATA_B0	AE34	SB_DQ[0]	SB_MA[0]	AL19 M_MA_B0
M_DATA_B1	AE35	SB_DQ[1]	SB_MA[1]	AK23 M_MA_B1
M_DATA_B2	AG35	SB_DQ[2]	SB_MA[2]	AM22M_MA_B2
M_DATA_B3	AH35	SB_DQ[3]	SB_MA[3]	AM23M_MA_B3
M_DATA_B4	AD34	SB_DQ[4]	SB_MA[4]	AP23 M_MA_B4
M_DATA_B5	AD35	SB_DQ[5]	SB_MA[5]	AL23 M_MA_B5
M_DATA_B6	AG34	SB_DQ[6]	SB_MA[6]	AY24 M_MA_B6
M_DATA_B7	AH34	SB_DQ[7]	SB_MA[7]	AV25 M_MA_B7
M_DATA_B8	AL34	SB_DQ[8]	SB_MA[8]	AU26 M_MA_B8
M_DATA_B9	AL35	SB_DQ[9]	SB_MA[9]	AW25M_MA_B9
M_DATA_B10	AK31	SB_DQ[10]	SB_MA[10]	AP18 M_MA_B10
M_DATA_B11	AL31	SB_DQ[11]	SB_MA[11]	AY25 M_MA_B11
M_DATA_B12	AK34	SB_DQ[12]	SB_MA[12]	AV26 M_MA_B12
M_DATA_B13	AK35	SB_DQ[13]	SB_MA[13]	AR15 M_MA_B13
M_DATA_B14	AK32	SB_DQ[14]	SB_MA[14]	AV27 M_MA_B14
M_DATA_B15	AL32	SB_DQ[15]	SB_MA[15]	AY28 M_MA_B15
M_DATA_B16	AN34	SB_DQ[16]	SB_ODT[0]	AM17M_ODT_B0
M_DATA_B17	AP34	SB_DQ[17]	SB_ODT[1]	AL16 M_ODT_B1
M_DATA_B18	AN31	SB_DQ[18]	SB_ODT[2]	AK15
M_DATA_B19	AP31	SB_DQ[19]	SB_ODT[3]	AK15
M_DATA_B20	AN35	SB_DQ[20]	SB_ODT[4]	AK15
M_DATA_B21	AP35	SB_DQ[21]	SB_ODT[5]	AK15
M_DATA_B22	AN32	SB_DQ[22]	SB_ECC_CB[0]	AM26
M_DATA_B23	AP32	SB_DQ[23]	SB_ECC_CB[1]	AM25
M_DATA_B24	AM29	SB_DQ[24]	SB_ECC_CB[2]	AP25
M_DATA_B25	AM28	SB_DQ[25]	SB_ECC_CB[3]	AP26
M_DATA_B26	AR29	SB_DQ[26]	SB_ECC_CB[4]	AL26
M_DATA_B27	AR28	SB_DQ[27]	SB_ECC_CB[5]	AL25
M_DATA_B28	AL29	SB_DQ[28]	SB_ECC_CB[6]	AR26
M_DATA_B29	AL28	SB_DQ[29]	SB_ECC_CB[7]	AR25
M_DATA_B30	AP29	SB_DQ[30]		
M_DATA_B31	AP28	SB_DQ[31]		
M_DATA_B32	AL12	SB_DQ[32]	SB_BS[0]	AK17 M_BS_B0
M_DATA_B33	AP12	SB_DQ[33]	SB_BS[1]	AL18 M_BS_B1
M_DATA_B34	AL13	SB_DQ[34]	SB_BS[2]	AW28M_BS_B2
M_DATA_B35	AL12	SB_DQ[35]		
M_DATA_B36	AR13	SB_DQ[36]	SB_CKE[0]	AW29M_CKE_B0
M_DATA_B37	AR13	SB_DQ[37]	SB_CKE[1]	AW29M_CKE_B1
M_DATA_B38	AM13	SB_DQ[38]	SB_CKE[2]	AU28
M_DATA_B39	AM12	SB_DQ[39]	SB_CKE[3]	AU29
M_DATA_B40	AR9	SB_DQ[40]		
M_DATA_B41	AP9	SB_DQ[41]		
M_DATA_B42	AR6	SB_DQ[42]		
M_DATA_B43	AP6	SB_DQ[43]		
M_DATA_B44	AR10	SB_DQ[44]		
M_DATA_B45	AP10	SB_DQ[45]	SB_CS[0]	AP17 M_CS_B_L0
M_DATA_B46	AR7	SB_DQ[46]	SB_CS[1]	AN15 M_CS_B_L1
M_DATA_B47	AP7	SB_DQ[47]	SB_CS[2]	AN17
M_DATA_B48	AM9	SB_DQ[48]	SB_CS[3]	AL15
M_DATA_B49	AL9	SB_DQ[49]		
M_DATA_B50	AL6	SB_DQ[50]	SB_CK[0]	AM20M_CLK_B_P0
M_DATA_B51	AL7	SB_DQ[51]	SB_CK[0]	AM21M_CLK_B_N0
M_DATA_B52	AM10	SB_DQ[52]	SB_CK[1]	AP22 M_CLK_B_P1
M_DATA_B53	AL10	SB_DQ[53]	SB_CK[1]	AP21 M_CLK_B_N1
M_DATA_B54	AM6	SB_DQ[54]		
M_DATA_B55	AM7	SB_DQ[55]	SB_CK[2]	AN20
M_DATA_B56	AH6	SB_DQ[56]	SB_CK[2]	AN21
M_DATA_B57	AH7	SB_DQ[57]	SB_CK[3]	AP19
M_DATA_B58	AE6	SB_DQ[58]	SB_CK[3]	AP20
M_DATA_B59	AE7	SB_DQ[59]		
M_DATA_B60	AJ6	SB_DQ[60]	SB_CAS	AP16 M_CAS_B_L
M_DATA_B61	AJ7	SB_DQ[61]	RSVD_AL20	AL20 CPU_AL20
M_DATA_B62	AF6	SB_DQ[62]	SB_RAS	AM18M_RAS_B_L
M_DATA_B63	AF7	SB_DQ[63]	SB_WE	AK16 M_WE_B_L
M_DQS_B_P0	AF35	SB_DQS[0]	SA_DIMM_VREFDQ	AB39 DIMM_DQ_CPU
M_DQS_B_P1	AL33	SB_DQS[1]	SB_DIMM_VREFDQ	AB40 DIMM_DQ_CPU
M_DQS_B_P2	AP33	SB_DQS[2]		
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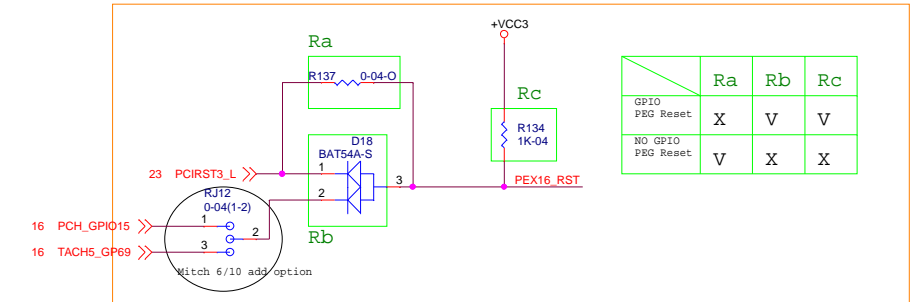

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**PCIE SPEC**
VCC3:3A
12V:5.5A
3VSB:0.375A
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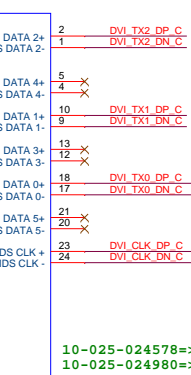
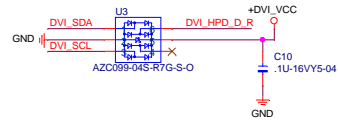
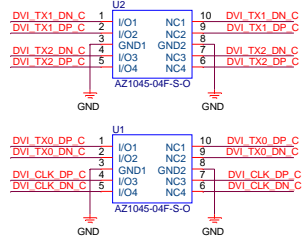
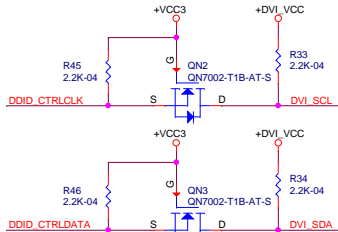
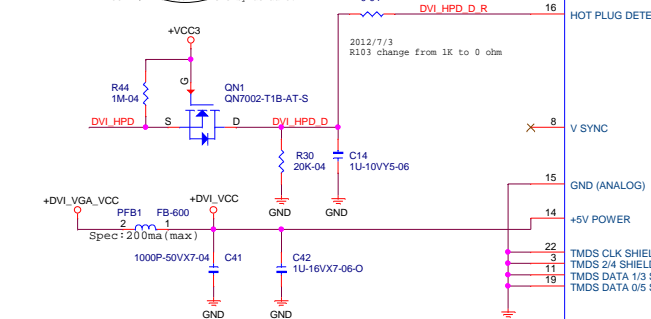
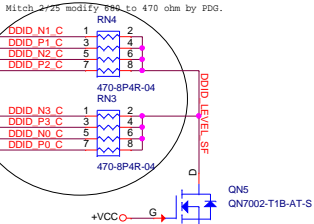
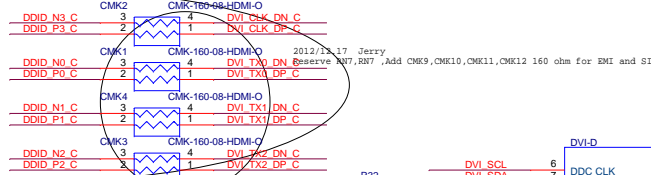
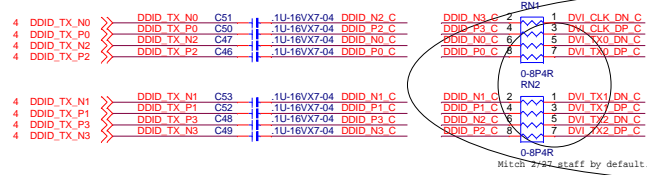
Between PCIEX16 & PCIEX1



報價先上,作Bom拿掉-Mitch



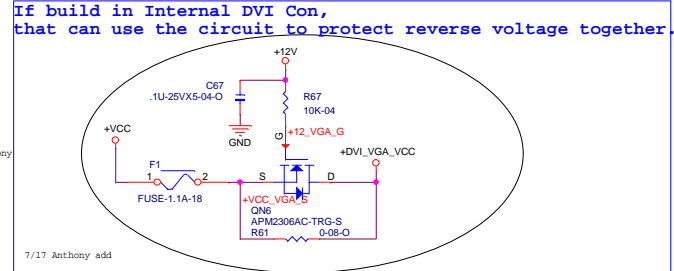
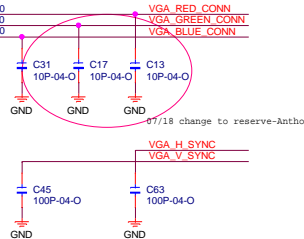
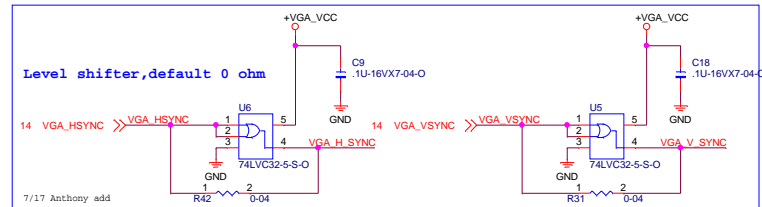
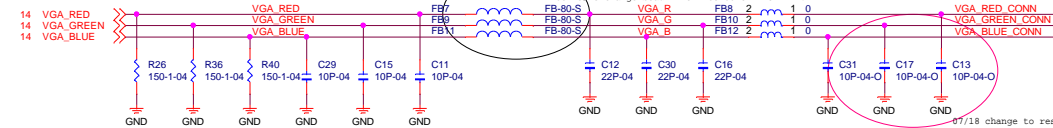
2012/7/05
PCIe Gen3 slot reset circuit update .



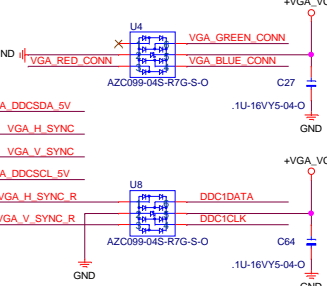
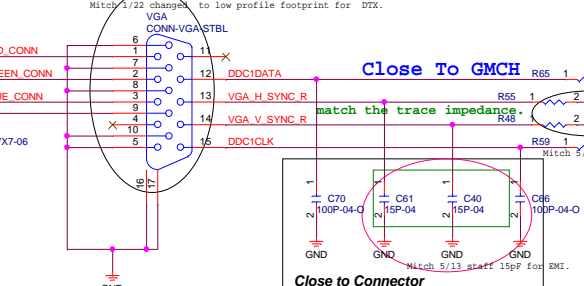
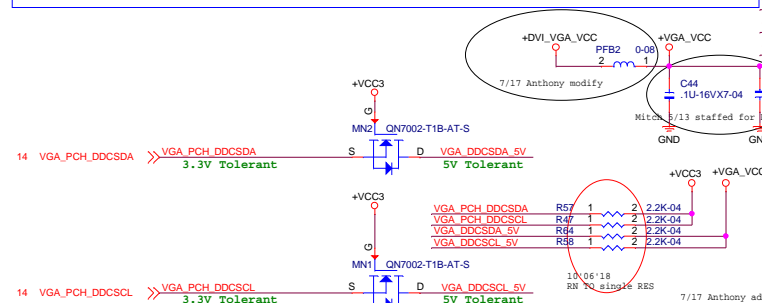
10-025-024578=>一般DVI port
10-025-024980=>多4个固定脚DVI

DVI-D

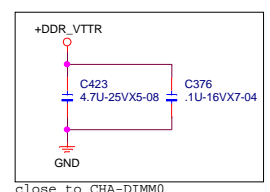
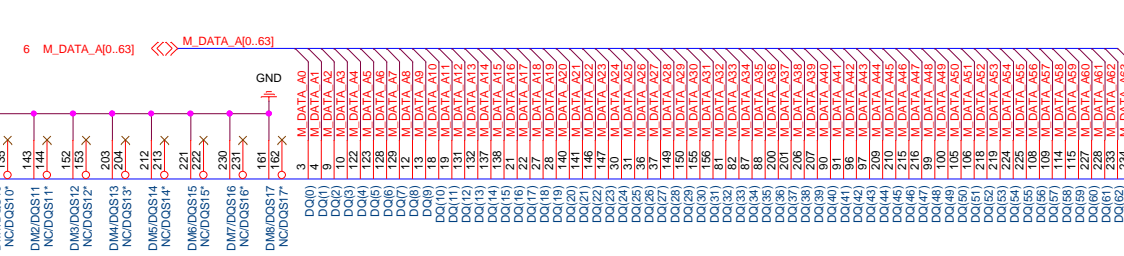
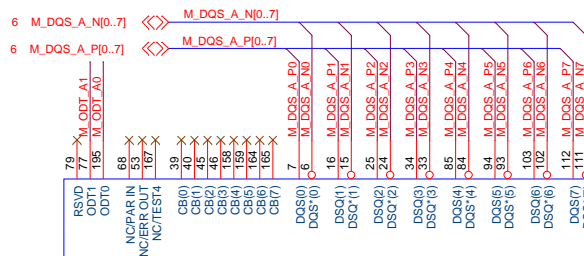
VGA



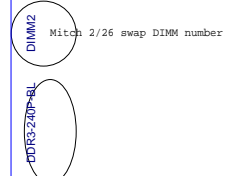
If build in Internal DVI Con, that can use the circuit to protect reverse voltage together.



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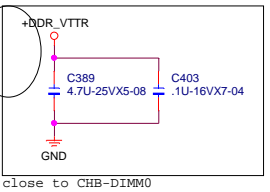
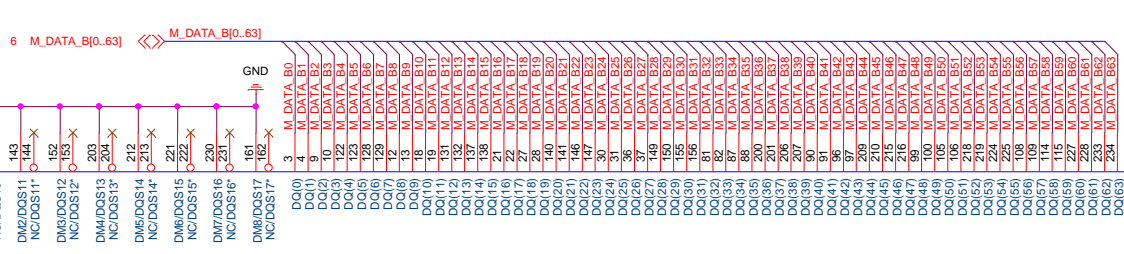
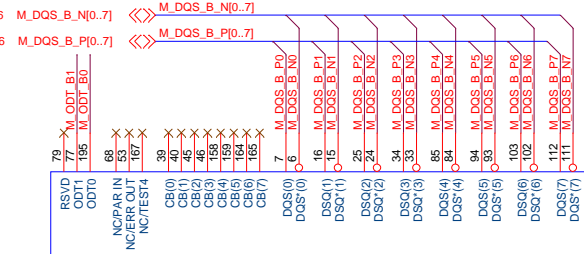
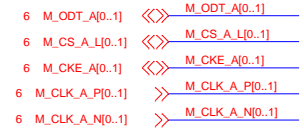
close to CHA-DIMM0



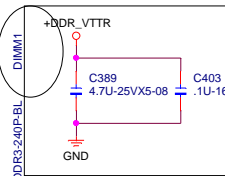
Mitch 2/26 swap DIMM number.

CHANNEL A DIMMs

2013/1/8 by nick change remove DIMM

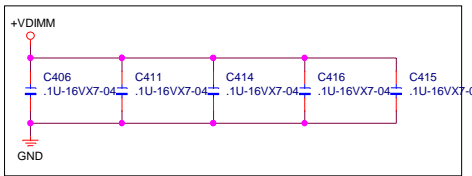


close to CHB-DIMM0

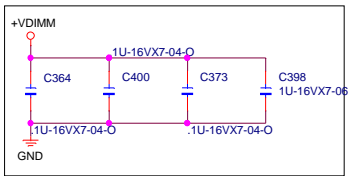


Mitch 2/26 swap DIMM number.

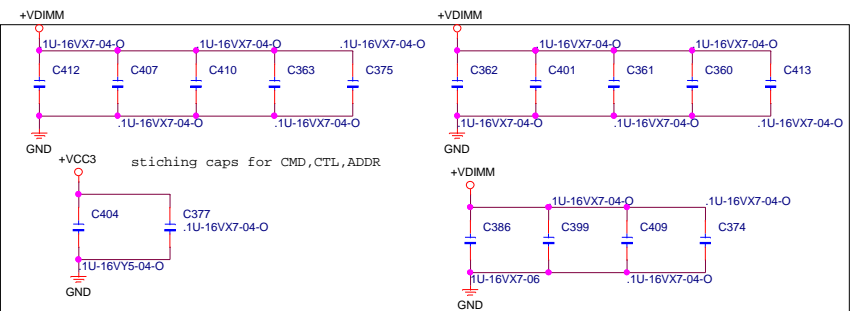
CHANNEL B DIMMs



close to CHA-DIMM2

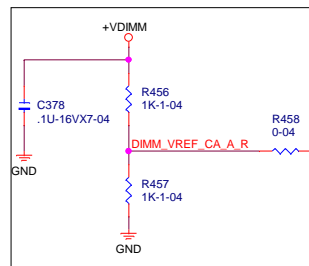


close to CHB-DIMM1

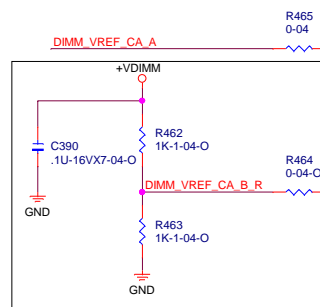


place between CHA&CHB
Don't punch VIAS

DDR3-CHA			
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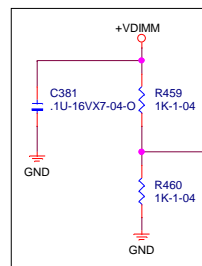
close to DIMM



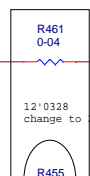
close to DIMM

0726 Fellow Intel PDG 1.0
VREF_CA Share-Anthony

DIMM_VREF_CA Circuit



close to DIMM's vref



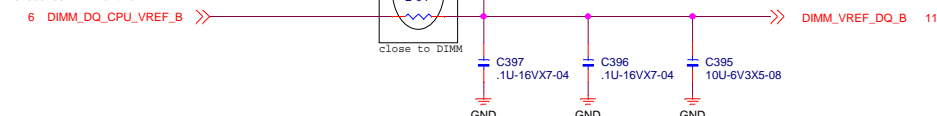
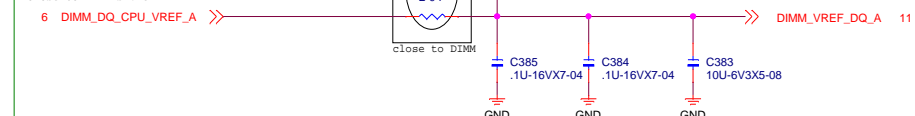
close to DIMM's vref

12'0328
change to 2 ohm (PN:05-152-200108)

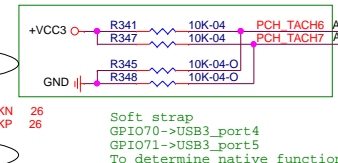
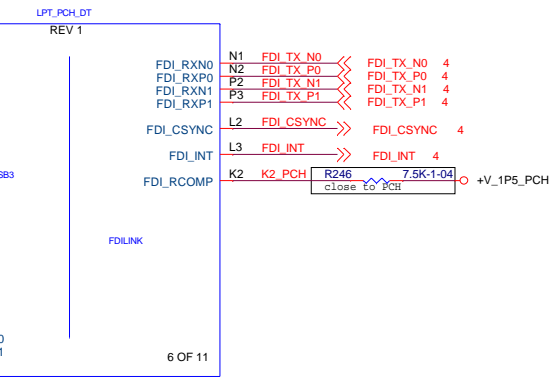
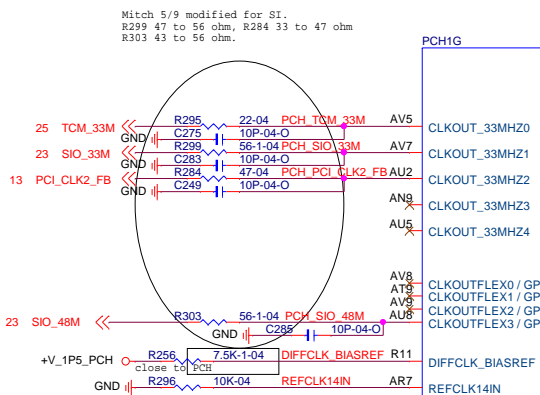
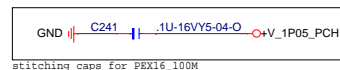
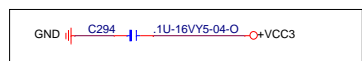
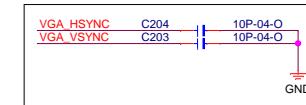
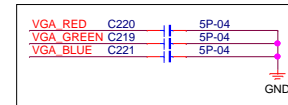
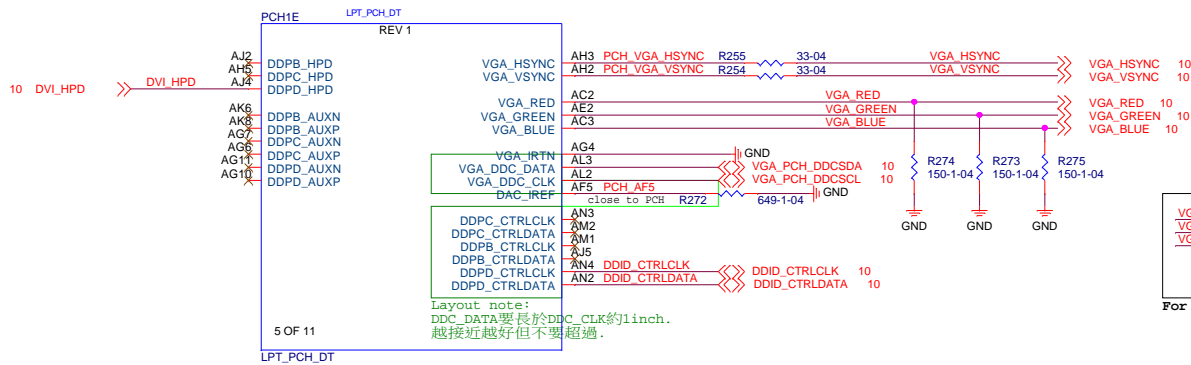
12'0328
change to 2 ohm (PN:05-152-200108)

close to DIMM

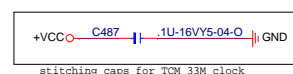
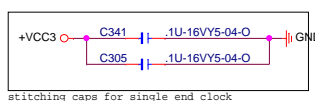
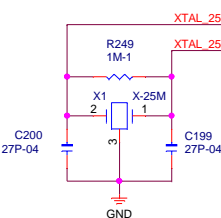
close to DIMM

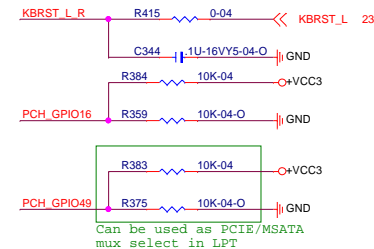
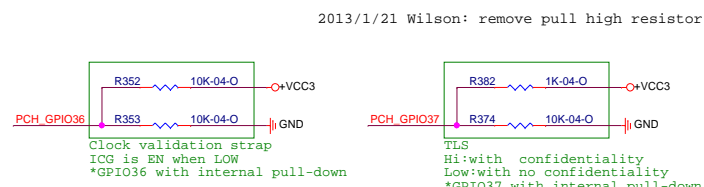
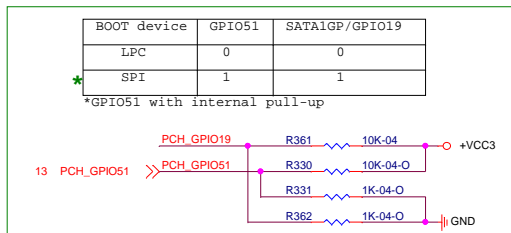
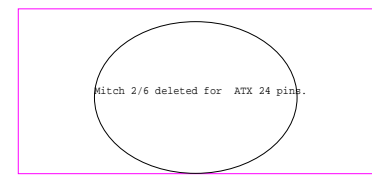
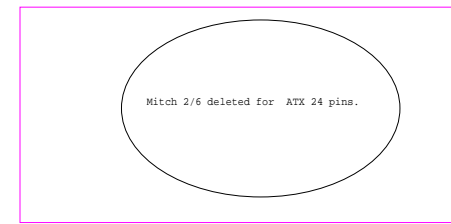
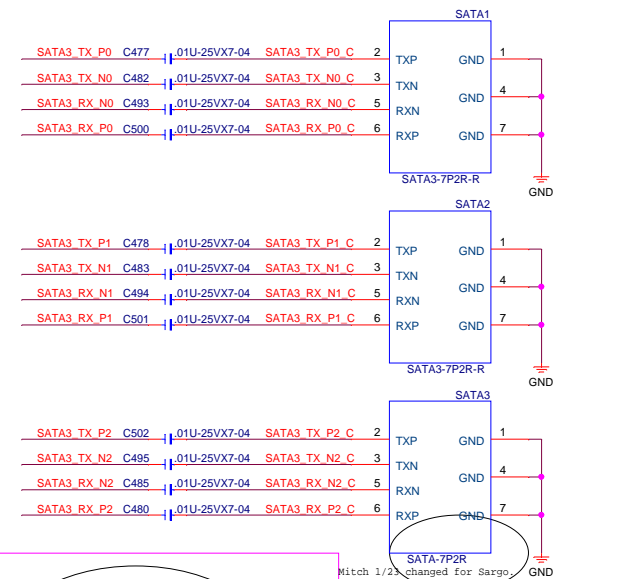
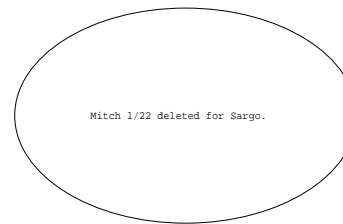
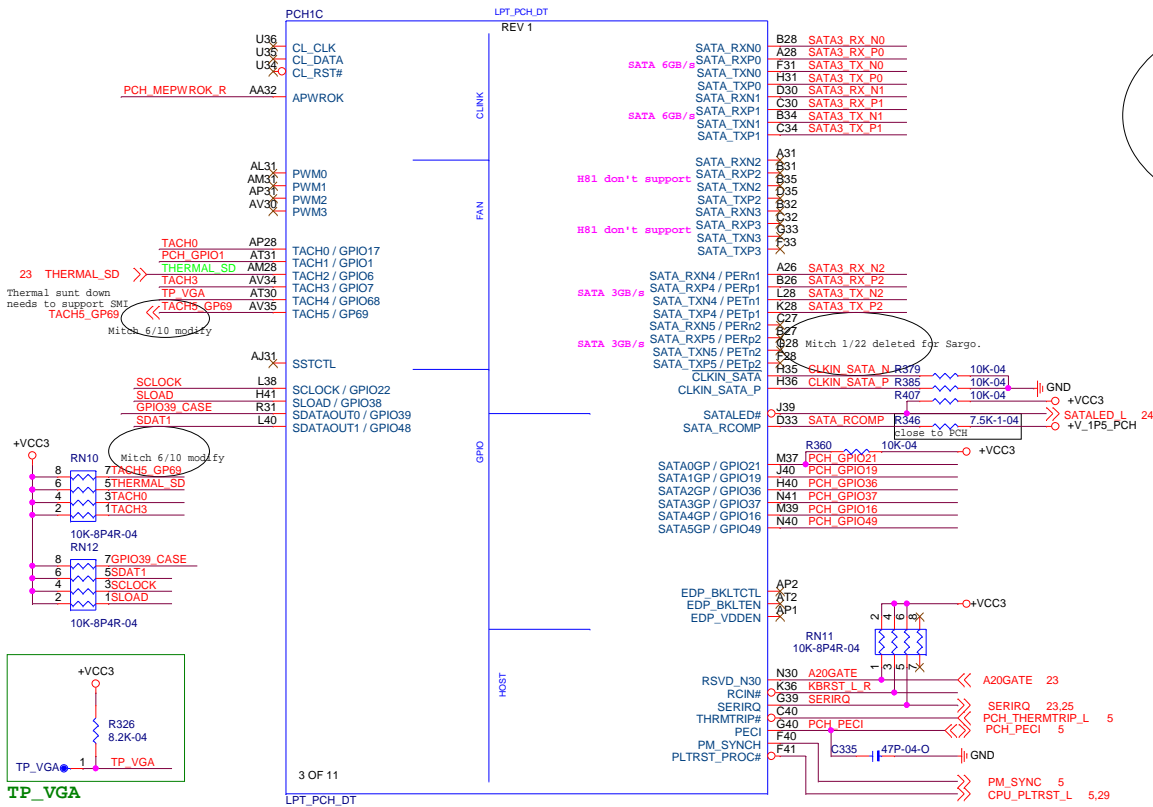


DIMM_VREF_DQ Circuit

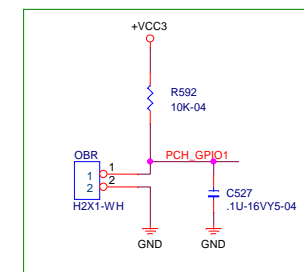


12/0203 WW051
N6/N7 pin swap

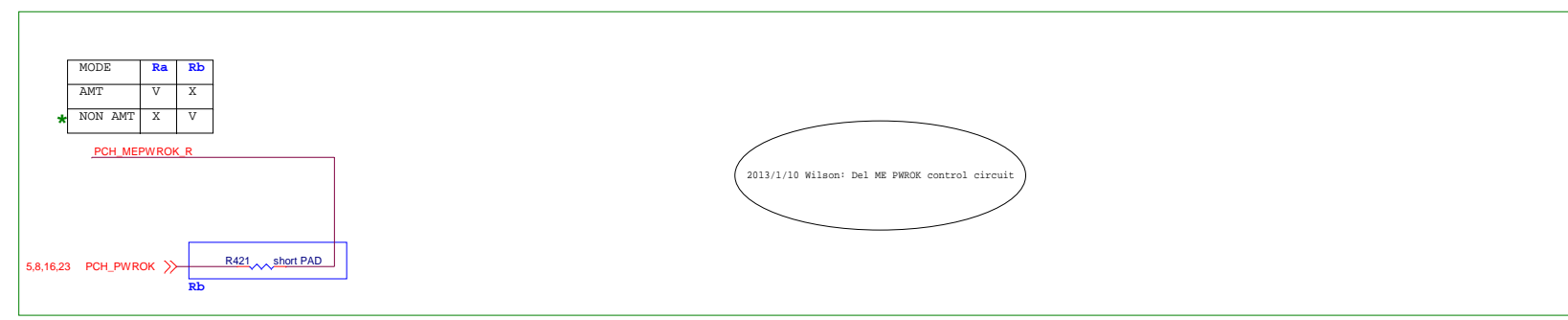




07/19 Chek need 2/3 PWR connector-Anthony

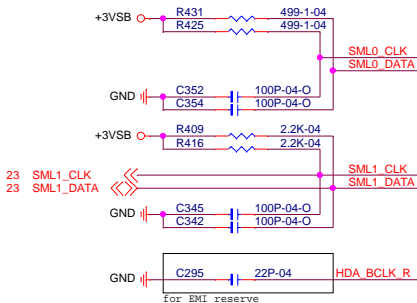
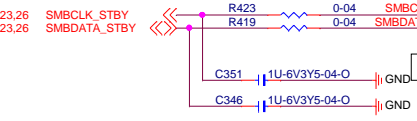
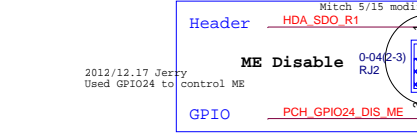
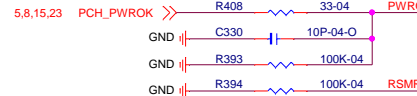
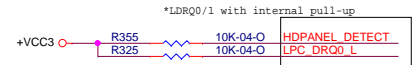


OBR header



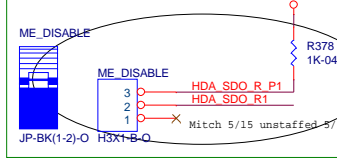
ME PWROK control circuit

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PCH-SATA/SATA connector/OBR			
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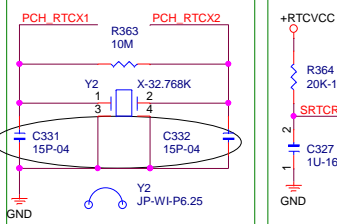


0726 reserve for Intel review Sonia-Anthony

MODE	SPI override
Disable ME	2-3
NORMAL	1-2

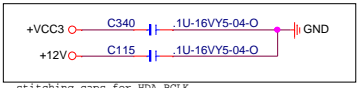
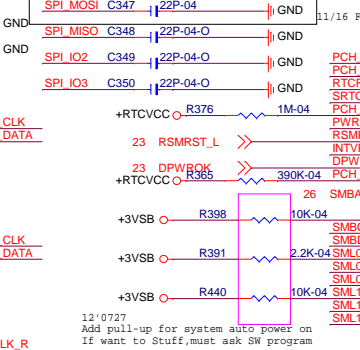
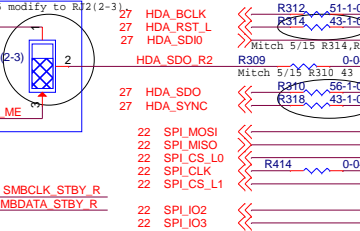
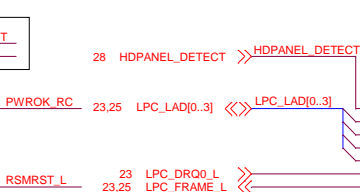


ME disable

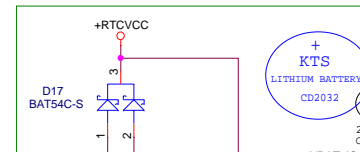
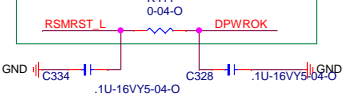


PCH Xtal

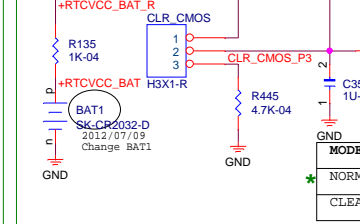
12/0528 C239 * C242 change to 15P for RTC test.



stitching caps for HDA_BCLK

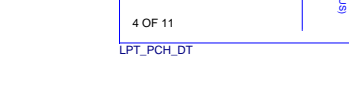
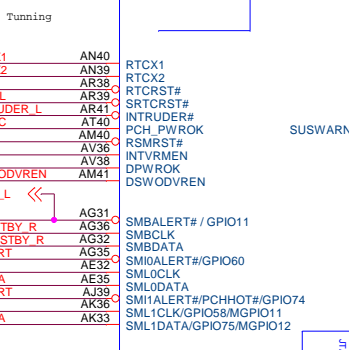
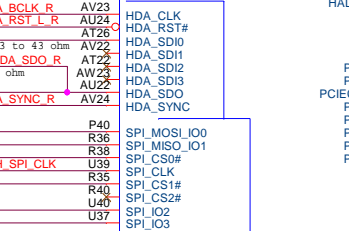
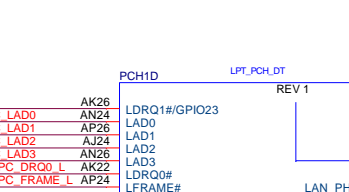


RTVC

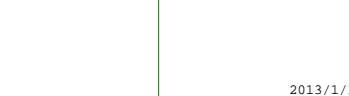


CLR CMOS

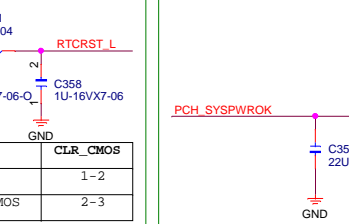
2012/07/09 Change BAT1



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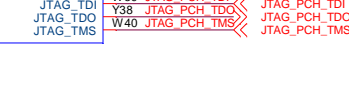
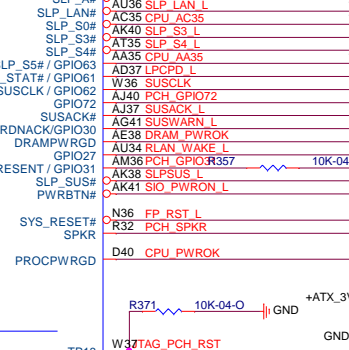
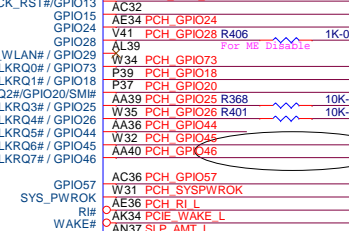
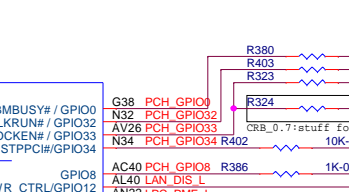


HSW Strap CFG13

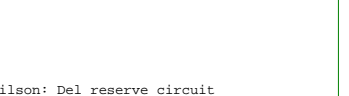


Reserve for Debug

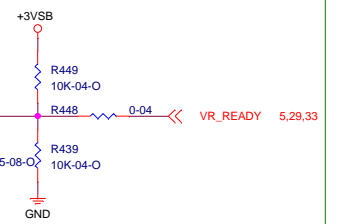
2013/1/18 Wilson: Del reserve circuit



2013/1/18 Wilson: Del reserve circuit

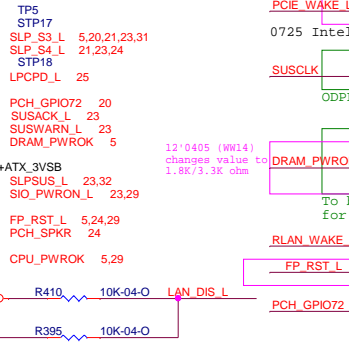
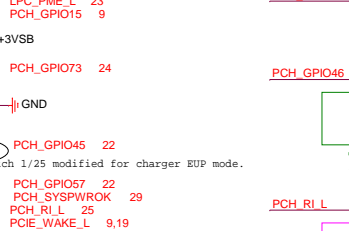


ME Disable

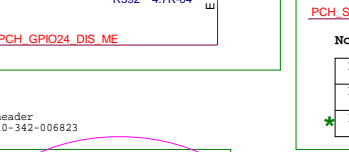
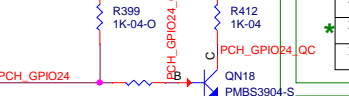


ME Test Header

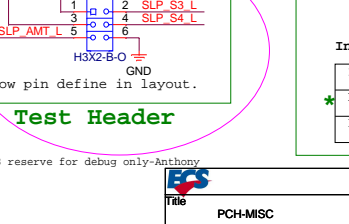
07/18 reserve for debug only-Anthony



2012/7/05 PCIe Gen3 slot reset circuit update.

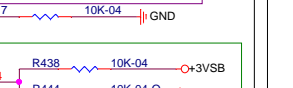
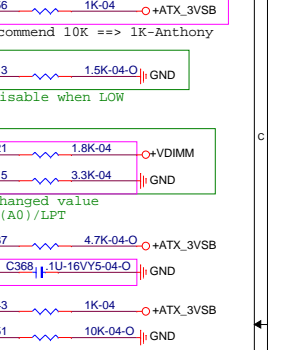
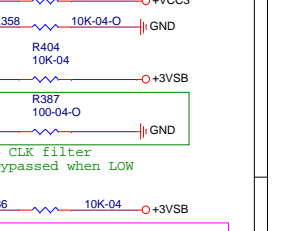
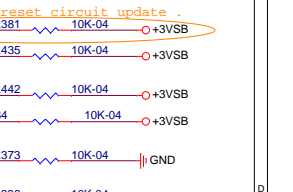


ME Disable

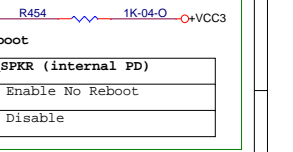
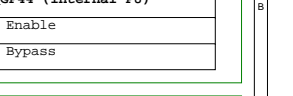


ME Test Header

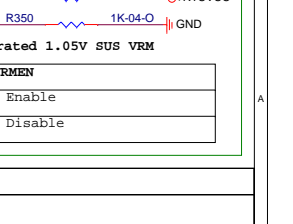
07/18 reserve for debug only-Anthony



2012/7/05 PCIe Gen3 slot reset circuit update.



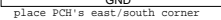
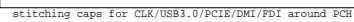
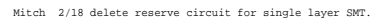
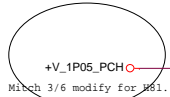
ME Disable

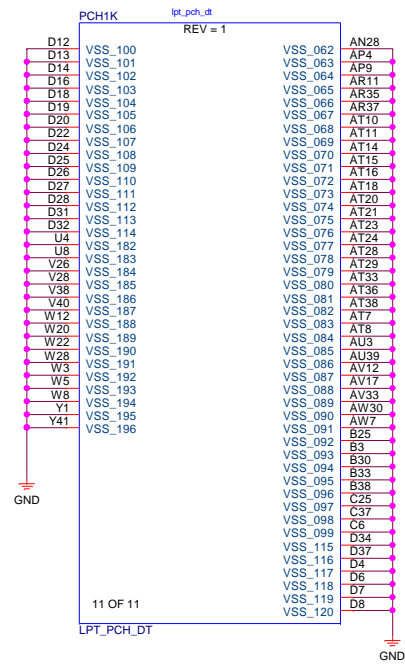
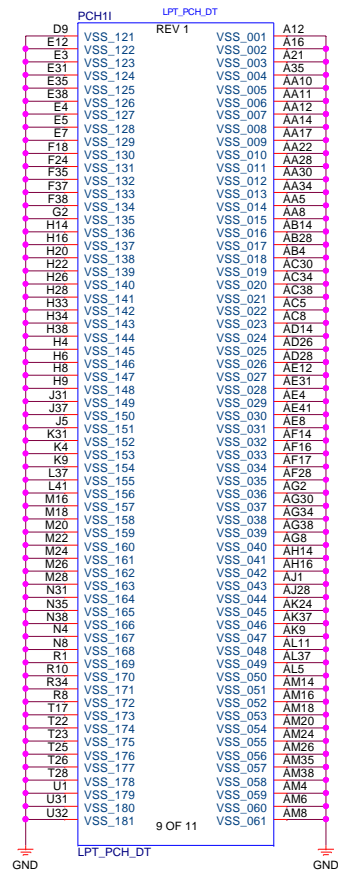
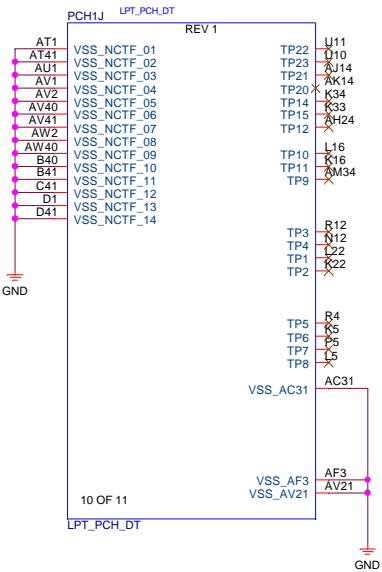


ME Test Header

07/18 reserve for debug only-Anthony

PCH-MISC			
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9,16,22,23,26 SMBCLK_STBY
9,16,22,23,26 SMBDATA_STBY
9,16 PCIE_WAKE_L

SMBCLK_STBY
SMBDATA_STBY
PCIE_WAKE_L

Mitch 1/22 deleted for Sargo.

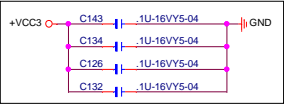
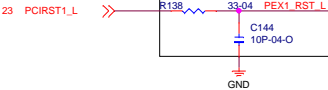
Mitch 1/22 deleted for Sargo.

2013/1/8 by nick change

14 PEX1_100M_P
14 PEX1_100M_N
13 PEX1_TX_P4
13 PEX1_TX_N4
13 PEX1_RX_P4
13 PEX1_RX_N4

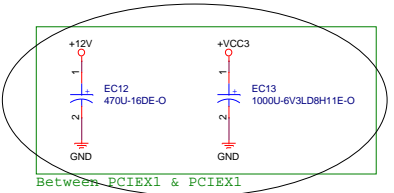
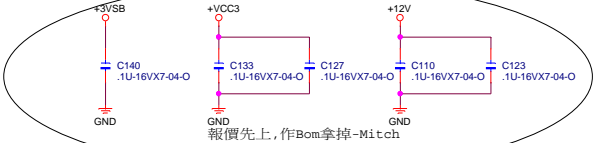
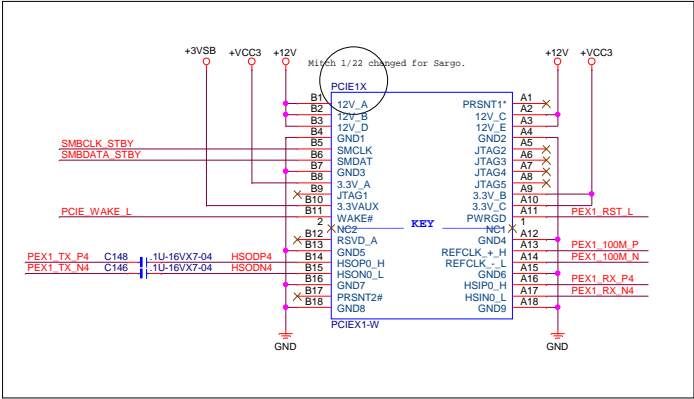
PEX1_100M_P
PEX1_100M_N
PEX1_TX_P4
PEX1_TX_N4
PEX1_RX_P4
PEX1_RX_N4

Mitch 1/22 deleted for Sargo.



stitching caps for 4X change reference layer

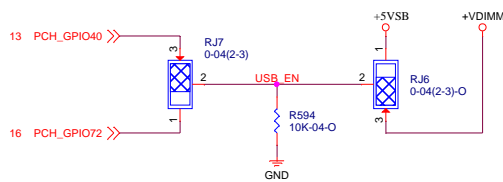
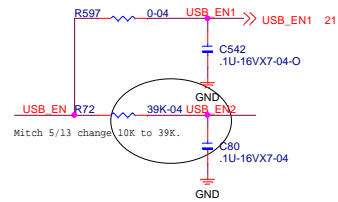
Mitch 1/22 deleted for Sargo.



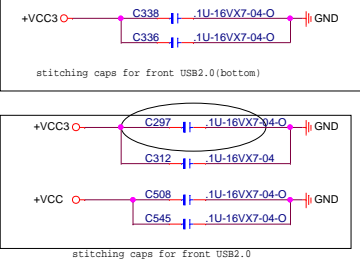
2013/1/18 報價不上-Mitch

報價先上, 作Bom拿掉-Anthony

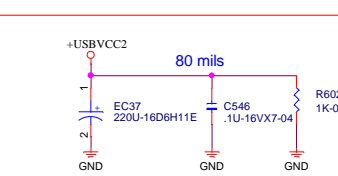
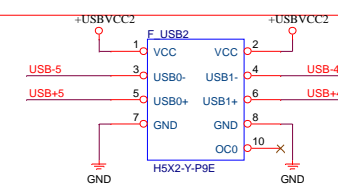
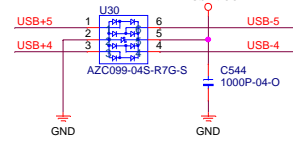
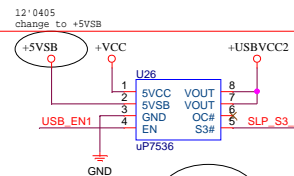
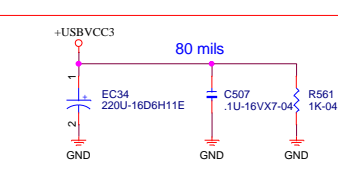
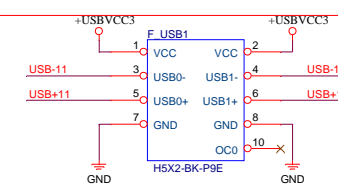
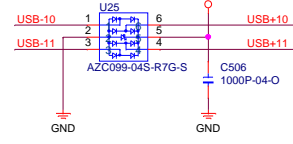
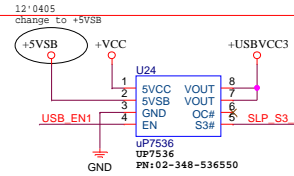
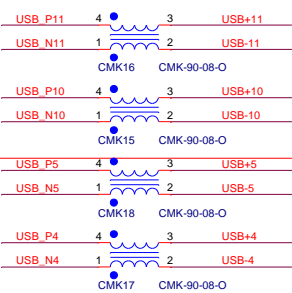
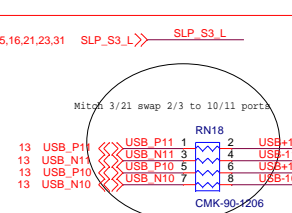
Title			
PCIE*4/PCIE*1			
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	uP7536 Enable use	RJ?	RJ?	S4/S5 USB_5V_DUAL	Customer
	VDIMM	0ohm (1-2)	NA	0 Volt	Acer S4 w/o S5 w/ USB_5VDUAL
	5VSB	0ohm (2-3)	NA	5 Volt	
*	GPIO	NA	0 ohm	S4 : 0 Volt S5 : 5 Volt	

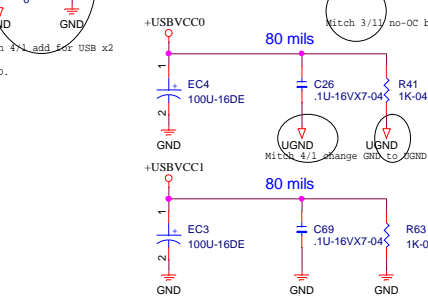
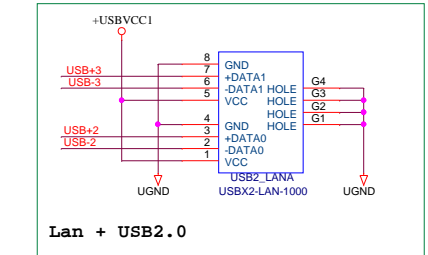
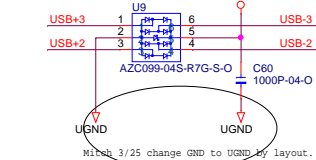
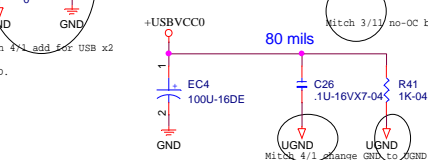
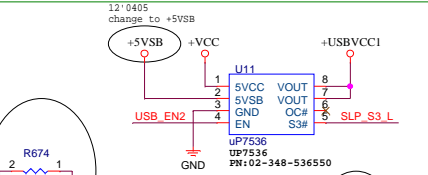
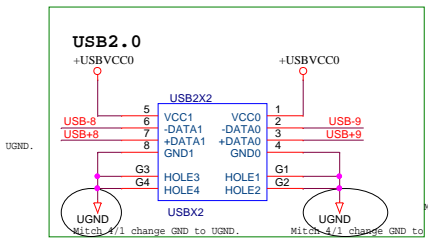
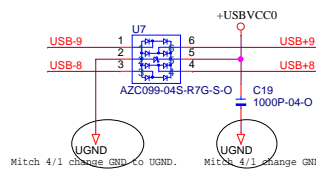
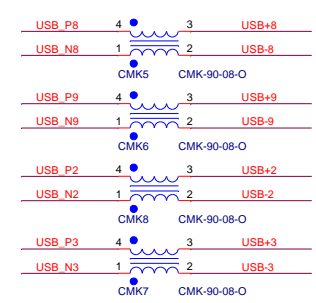
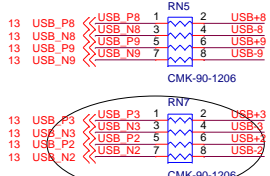


2013/1/9 Wilson Del_F_USB3, 單port



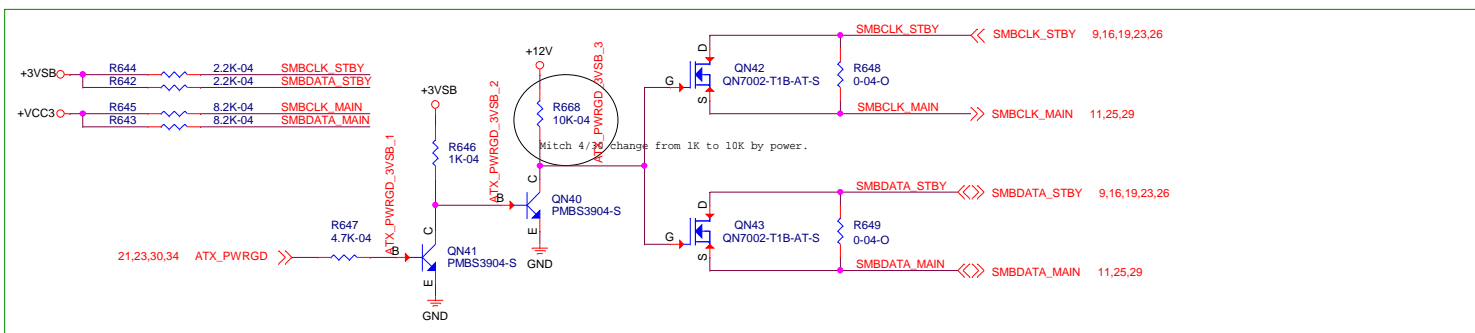
USB2.0 header

USB2.0 connector

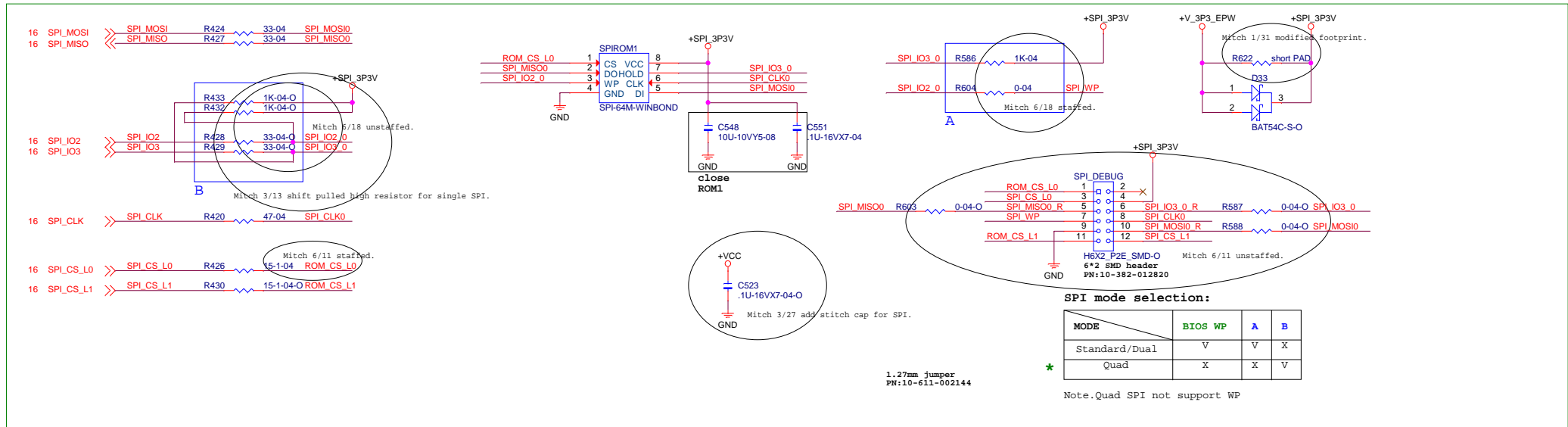


- OC[3:0]# should be connected with USB 2.0 ports 0 - 7 and any 4 of USB 3.0 ports 1 - 6.
- OC[7:4]# should be connected with USB 2.0 ports 8 - 13 and any 4 of USB 3.0 ports 1 - 6.

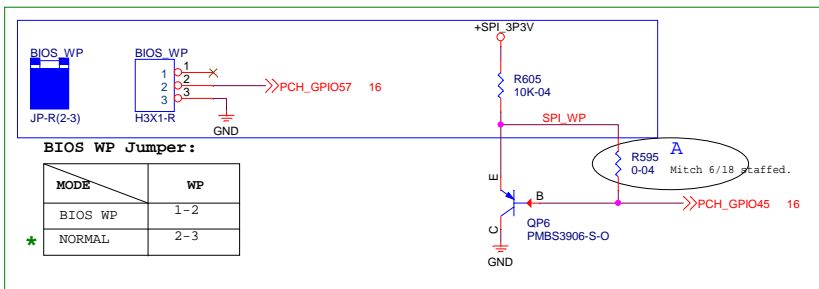
Title		
USB2.0 CONN & Header		
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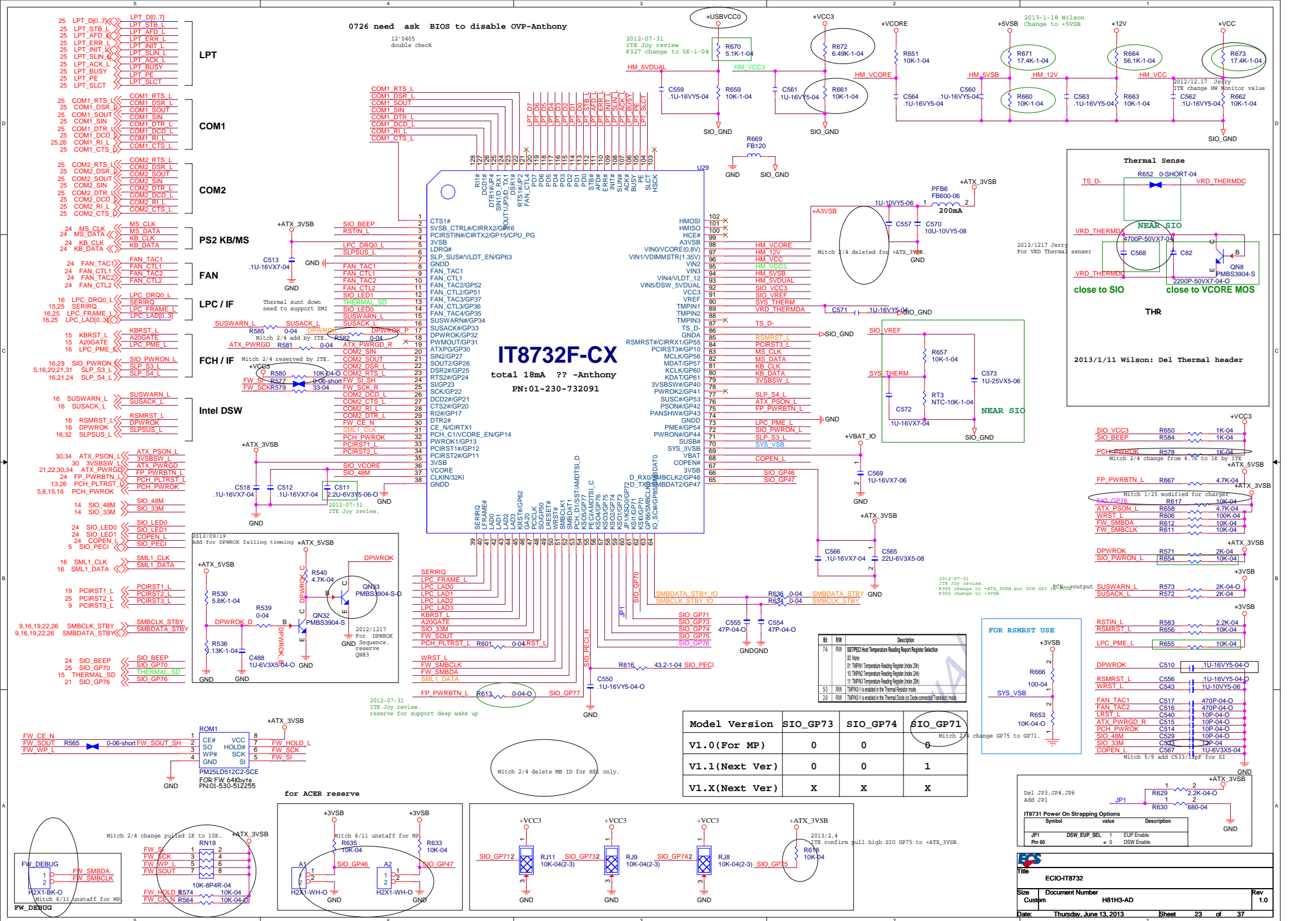
SMbus Logic Circuit

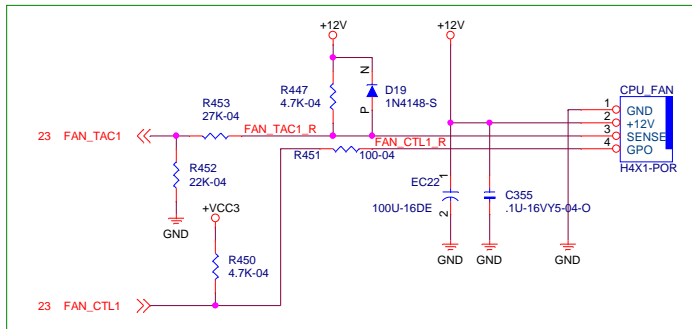


SPI ROM

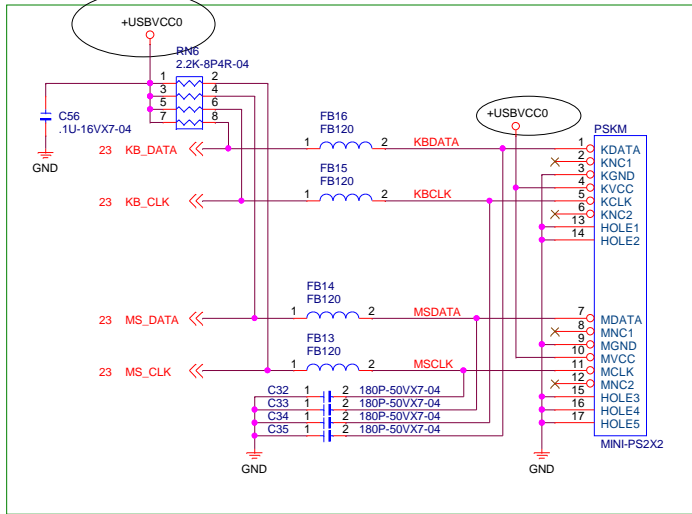


BIOS WP

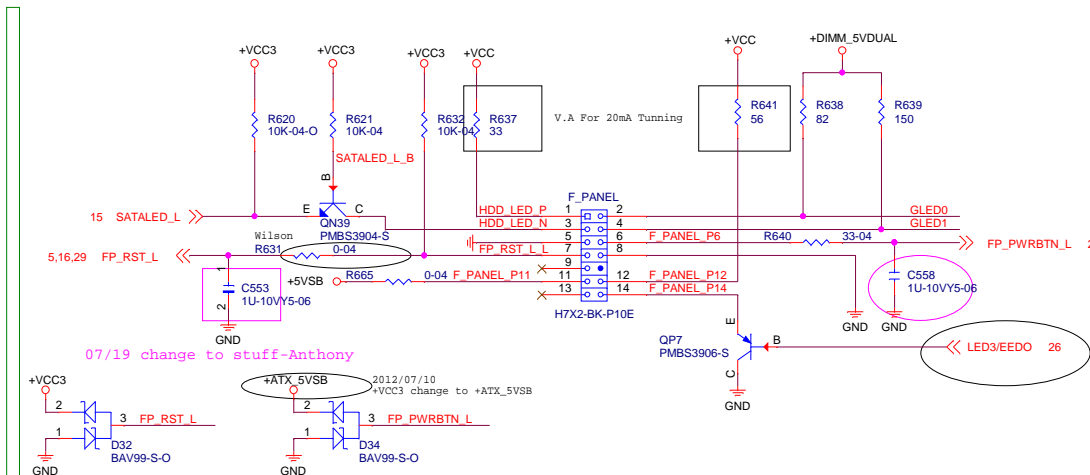




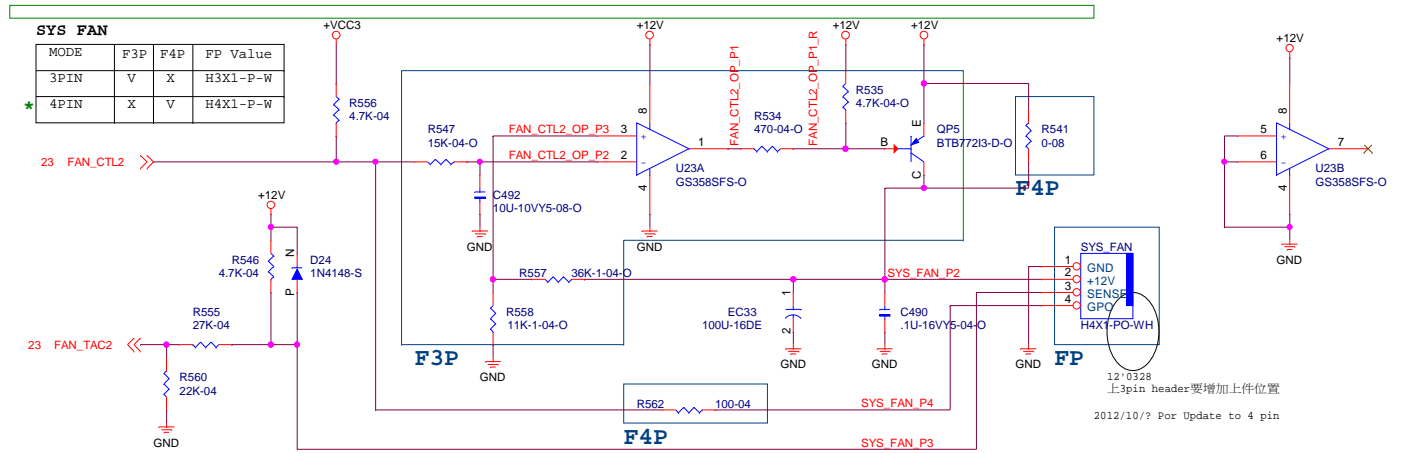
CPU_FAN 4 pin circuit



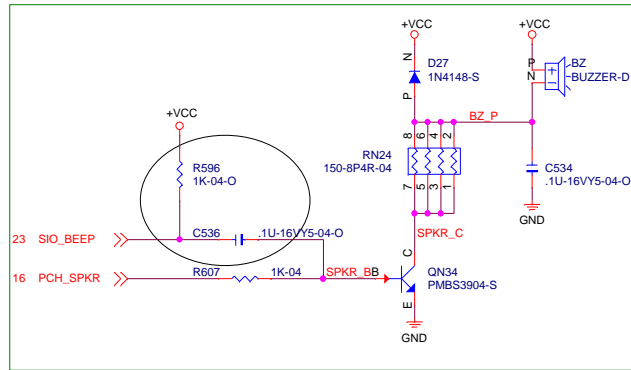
PS2 circuit



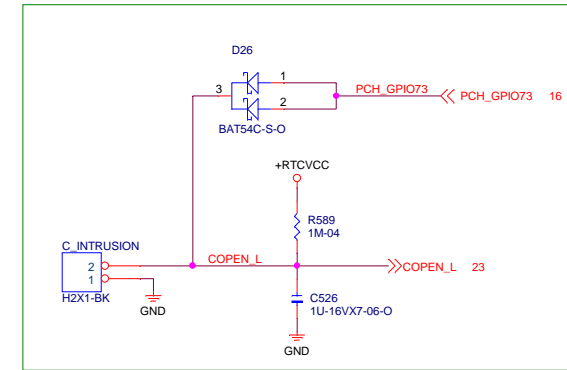
Front Panel circuit



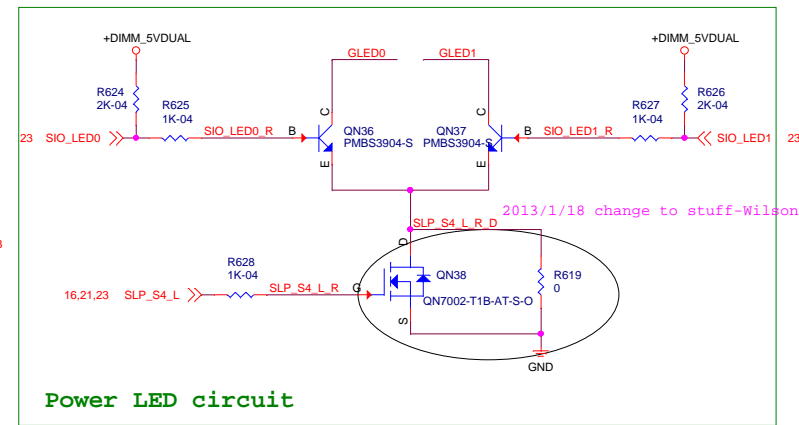
SYS_FAN 3/4 pin co-layout circuit



Buzzer circuit

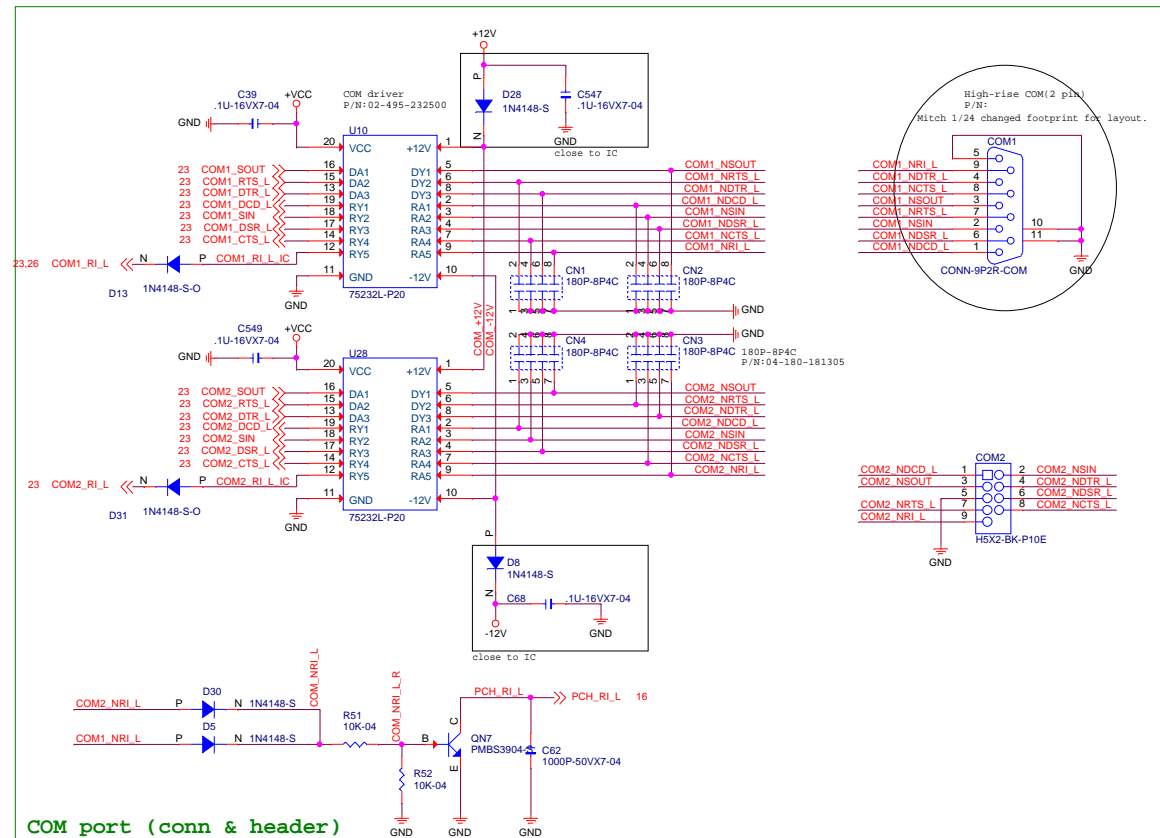
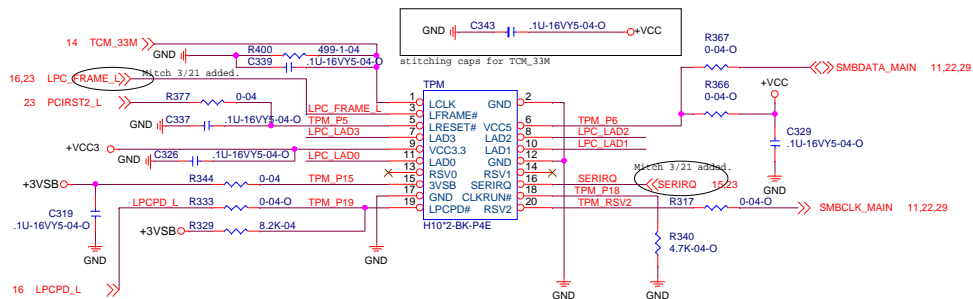
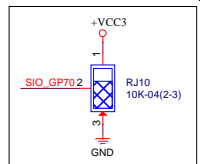
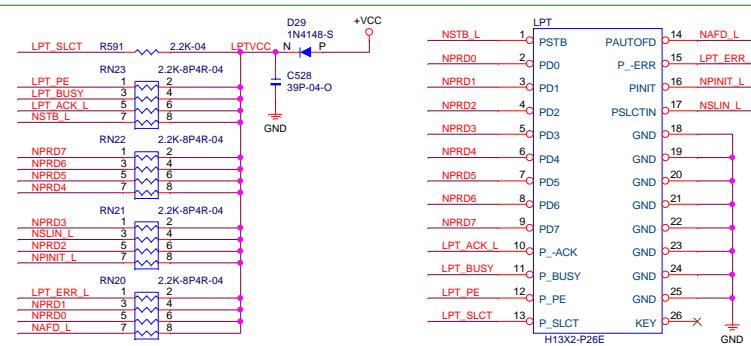



Case open circuit

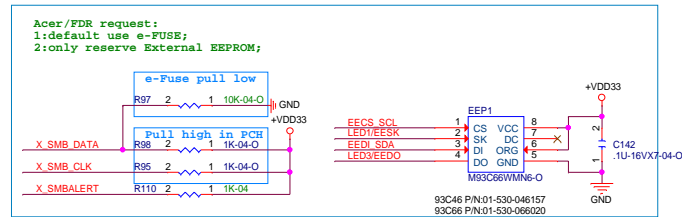
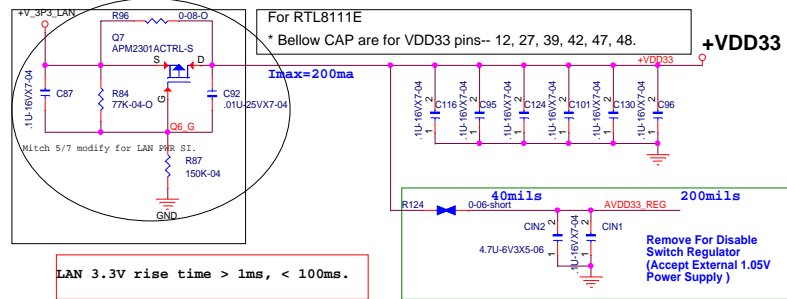


Power LED circuit

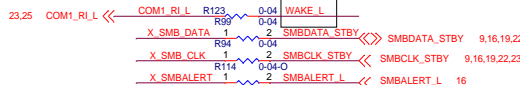
SIO_LED1 SIO_GP37	SIO_LED0 SIO_GP35	POWER LED
0 (low)	0 (low)	OFF
0 (low)	1 (High)	OFF
1 (High)	0 (low)	ON
1 (High)	1 (High)	OFF



				
Title				
LPT/COM/TPM				
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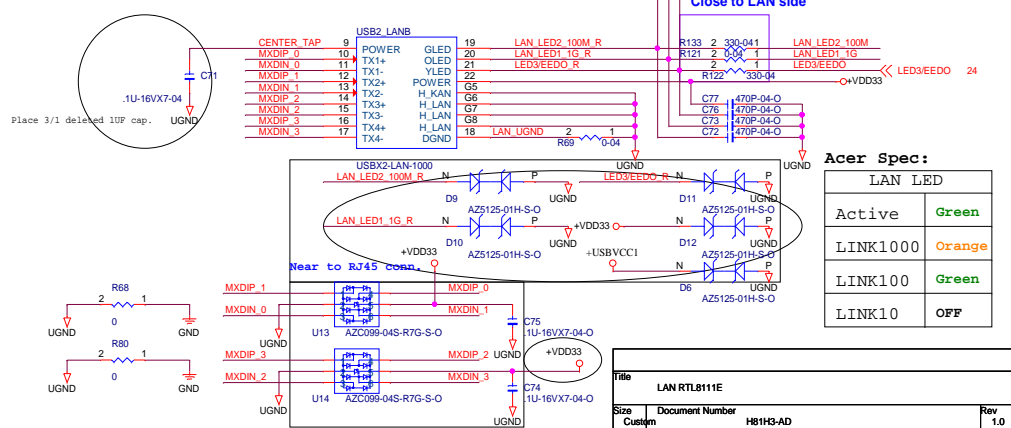
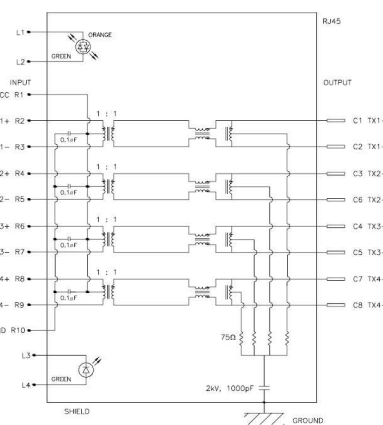
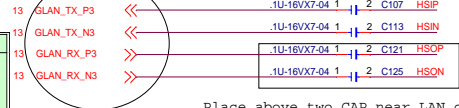
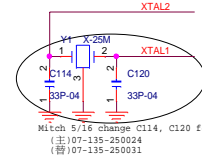
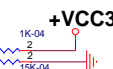
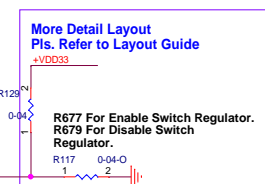
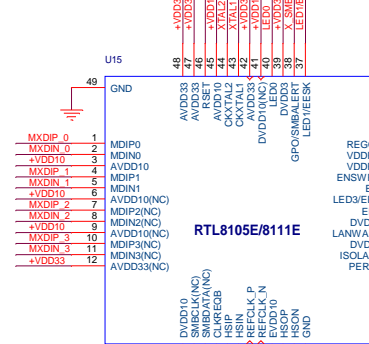
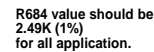
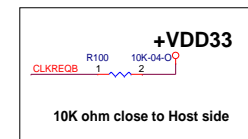
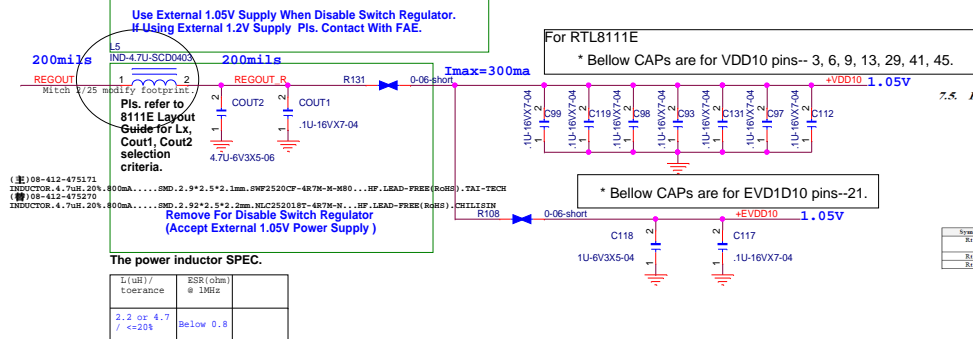
2013/1/18 Wilson: Link to RI to support G3 to S5



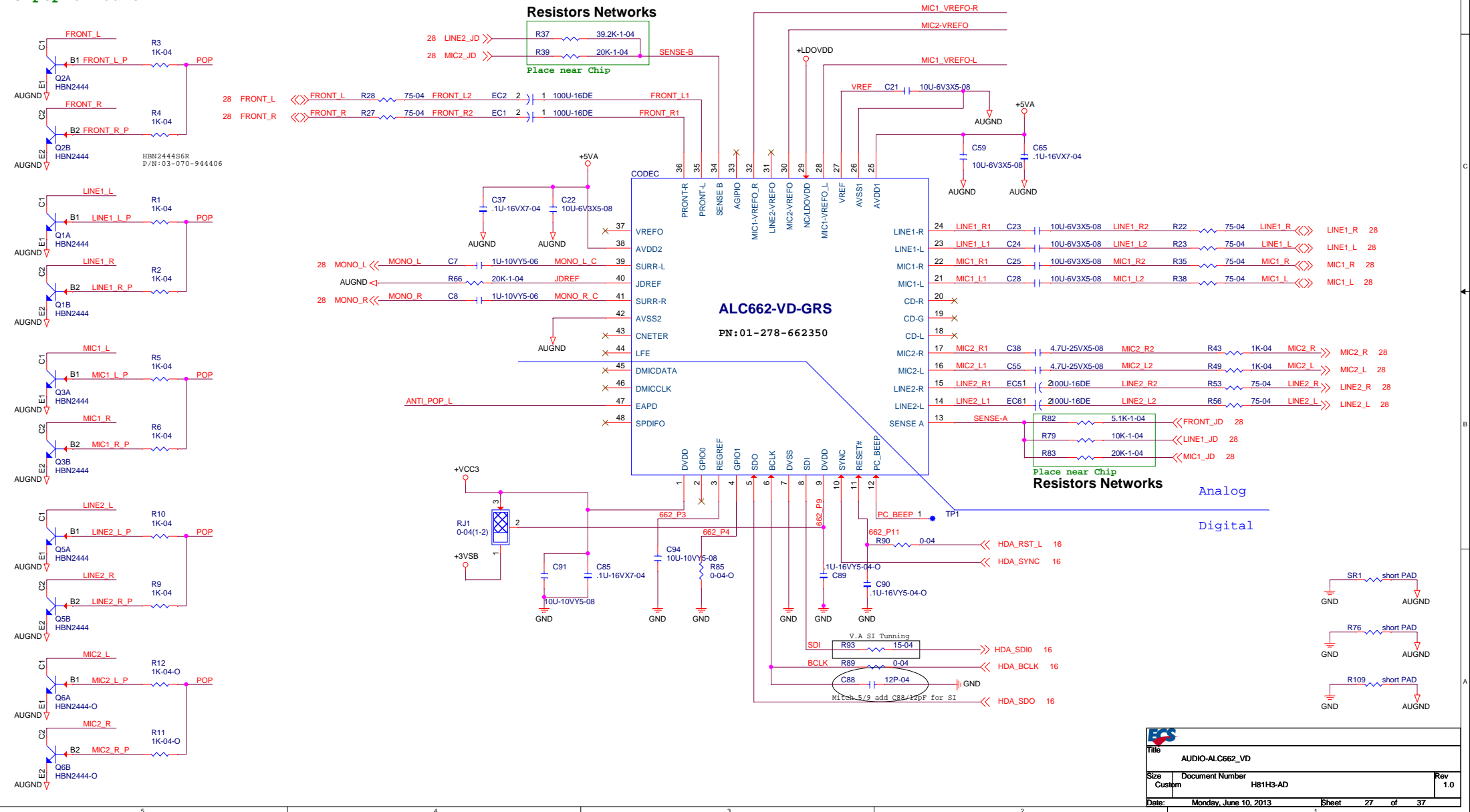
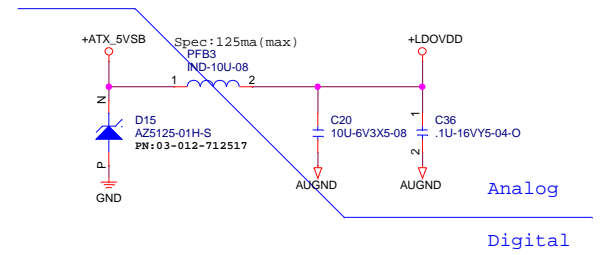
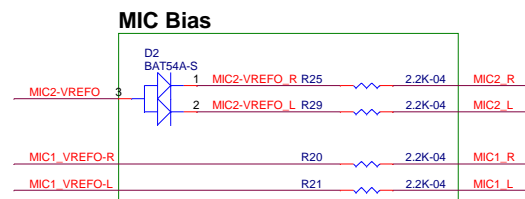
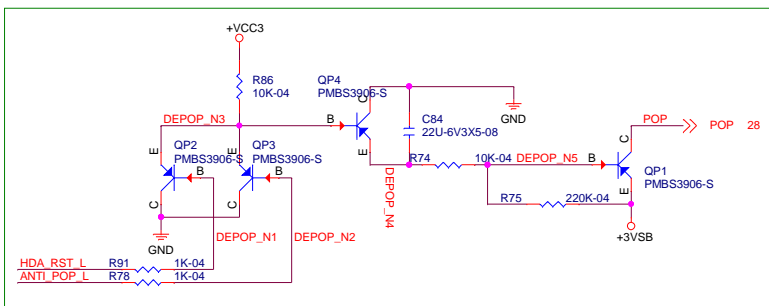
Acer Lan LED Status

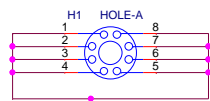
Wake on LAN (WOL) set to ON ==> In BIOS and OS									
	LED		S0	S1	S3	S4	S5	G3 to S5 unplug and plug power cord	
Rear Side	ACTIVE-LED (Single Color)	Access Blink	Blink	Blink	Blink	Blink	Blink	OFF	
		Others: OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
	SPEED-LED (Dual Color)	Disconnected: OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
		1000: ON with A color: Amber	Amber	OFF	OFF	OFF	OFF	OFF	OFF
		100: ON with B color: Green	Green	OFF	OFF	OFF	OFF	OFF	OFF
		10: OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
Front Side	(Single Color)	Access: Blinking Others: OFF	Access: Blinking Others: OFF	OFF		OFF	OFF	OFF	

Wake on LAN (WOL) set to OFF ==> In BIOS and OS								
	LED	S0	S0	S1	S3	S4	S5	G3 to S5 unplug and plug power cord
Rear Side	ACTIVE-LED (Single Color)	Access Blink	Blink	OFF	OFF	OFF	OFF	OFF
		Others OFF	OFF	OFF	OFF	OFF	OFF	OFF
	SPEED-LED (Dual Color)	Disconnected OFF	OFF	OFF	OFF	OFF	OFF	OFF
		1000: ON with A color: Amber	Amber	OFF	OFF	OFF	OFF	OFF
Front Side	(Single Color)	1000: ON with B color: Green	Green	OFF	OFF	OFF	OFF	OFF
		10: OFF	OFF	OFF	OFF	OFF	OFF	OFF
Front Side	(Single Color)	Access: Blinking Others: OFF	Access: Blinking Others: OFF	OFF	OFF	OFF	OFF	OFF
						OFF	OFF	OFF

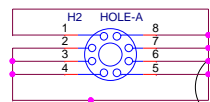


LAN LED	
Active	Green
LINK1000	Orange
LINK100	Green
LINK10	OFF

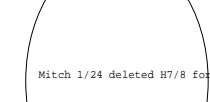
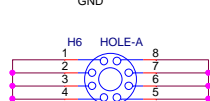
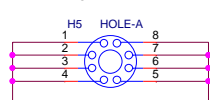
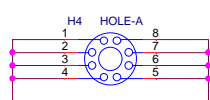
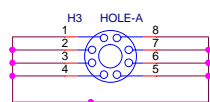




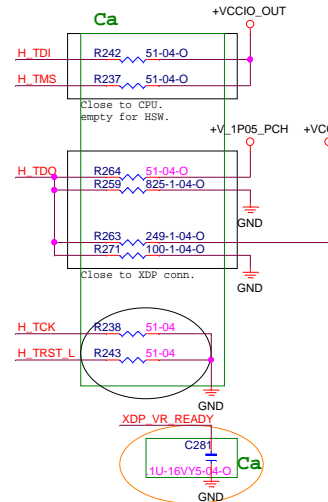
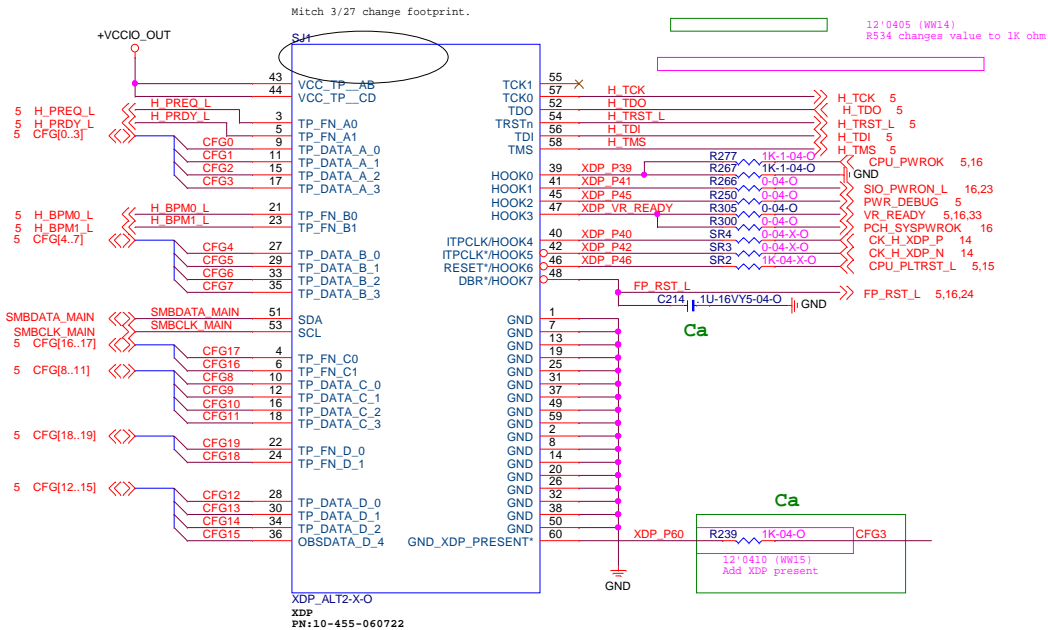
AUGND



Mitch 3/12 modified for H81.



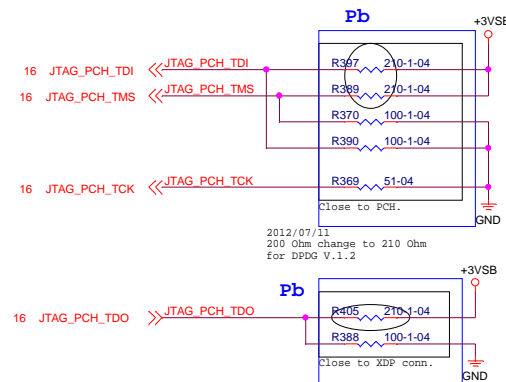
Mitch 1/24 deleted H7/8 for Sargo DTX.



12'0425 (CRB 1.0)
Add 0.1uF cap for ITP Hot plug fix

	Ca
CPU XDP function	V
NO CPU XDP function	X

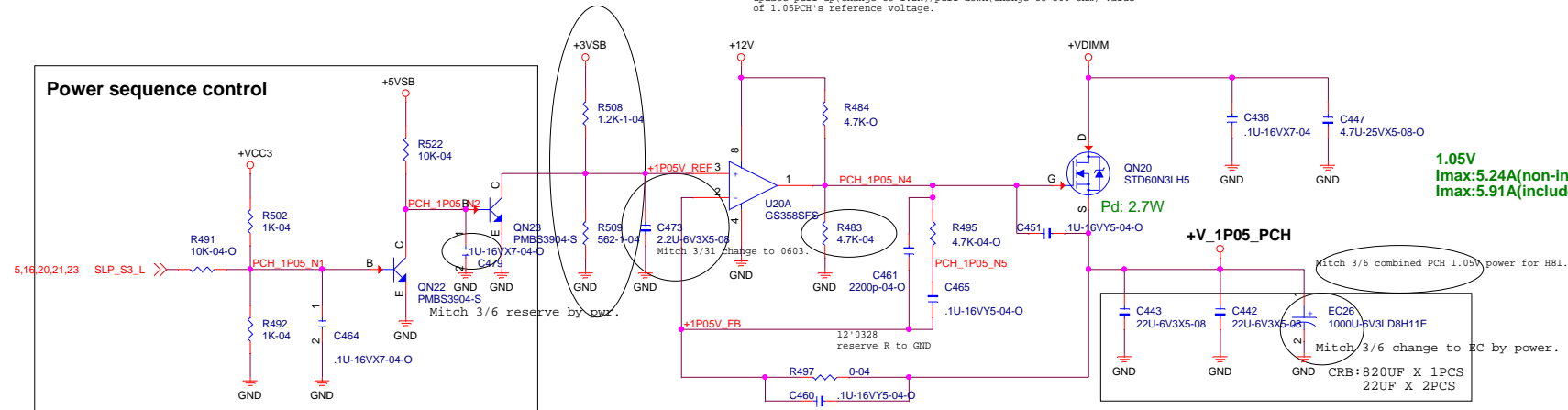
-0:報價



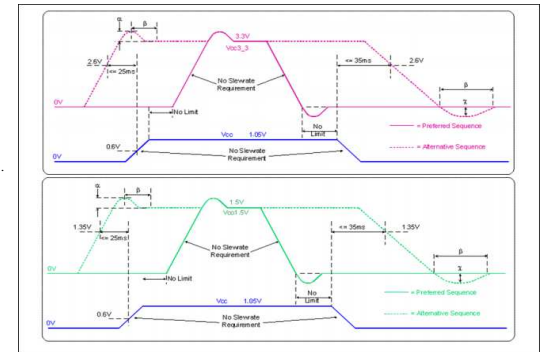
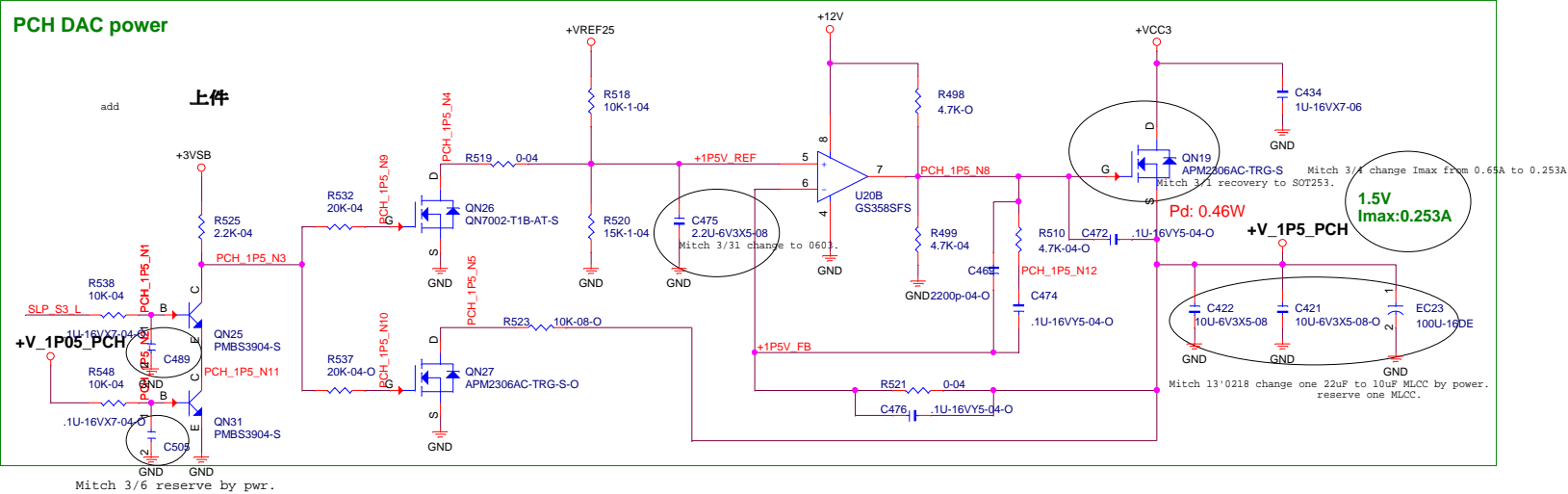
	Pb
PCH XDP function	V
NO PCH XDP function	X

PCH core power

12'0328
update pull-up(change to 1.2K)/pull-down(change to 560 ohm) value
of 1.05PCH's reference voltage.

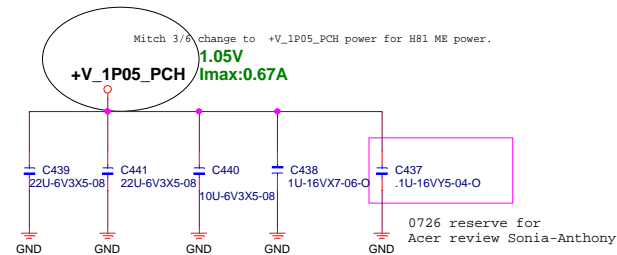


PCH DAC power



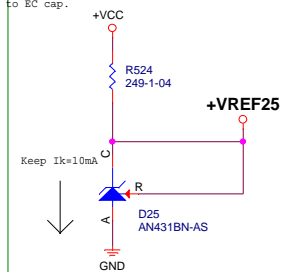
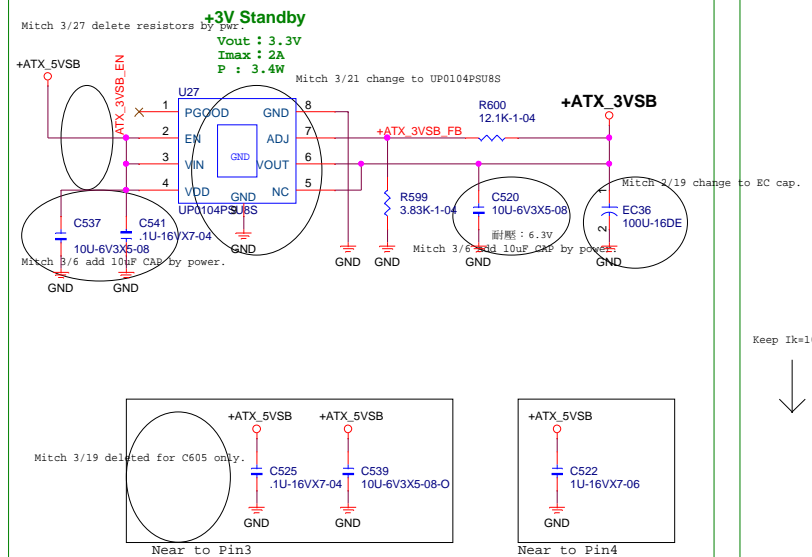
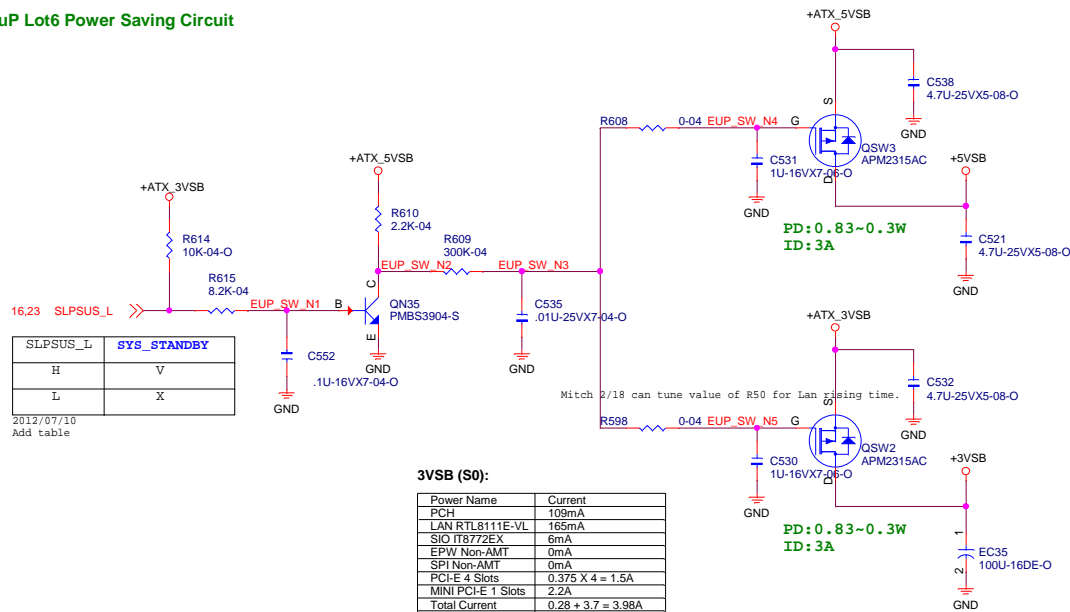
PCH ME power

2013/1/10 Wilson: Del ME POWER circuit

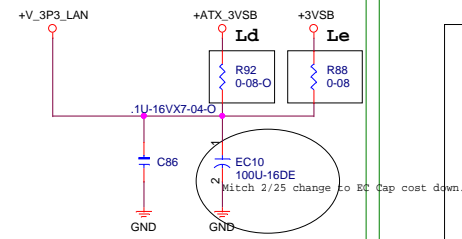
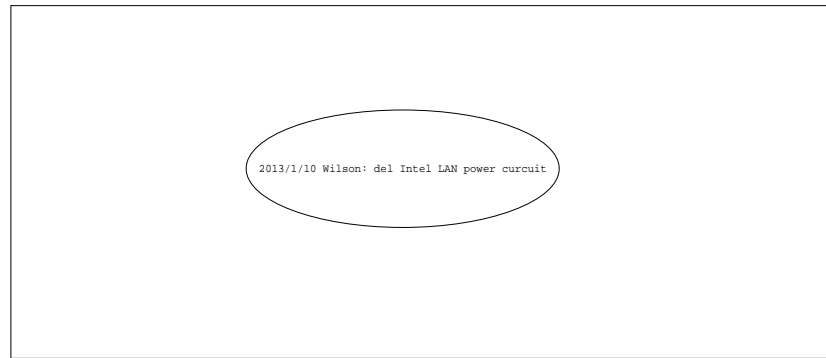


Title			DC/DC PCH_1.5V/PCH_ME_1.05V
Size	Document Number	Rev	
Custom	H81H3-AD	1.0	
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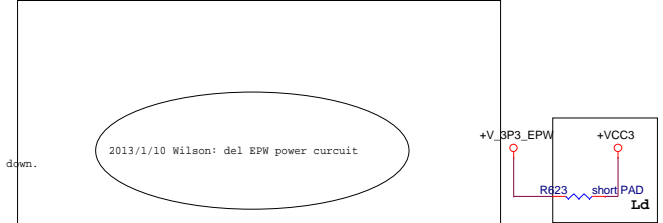
EuP Lot6 Power Saving Circuit



LAN Power Circuit



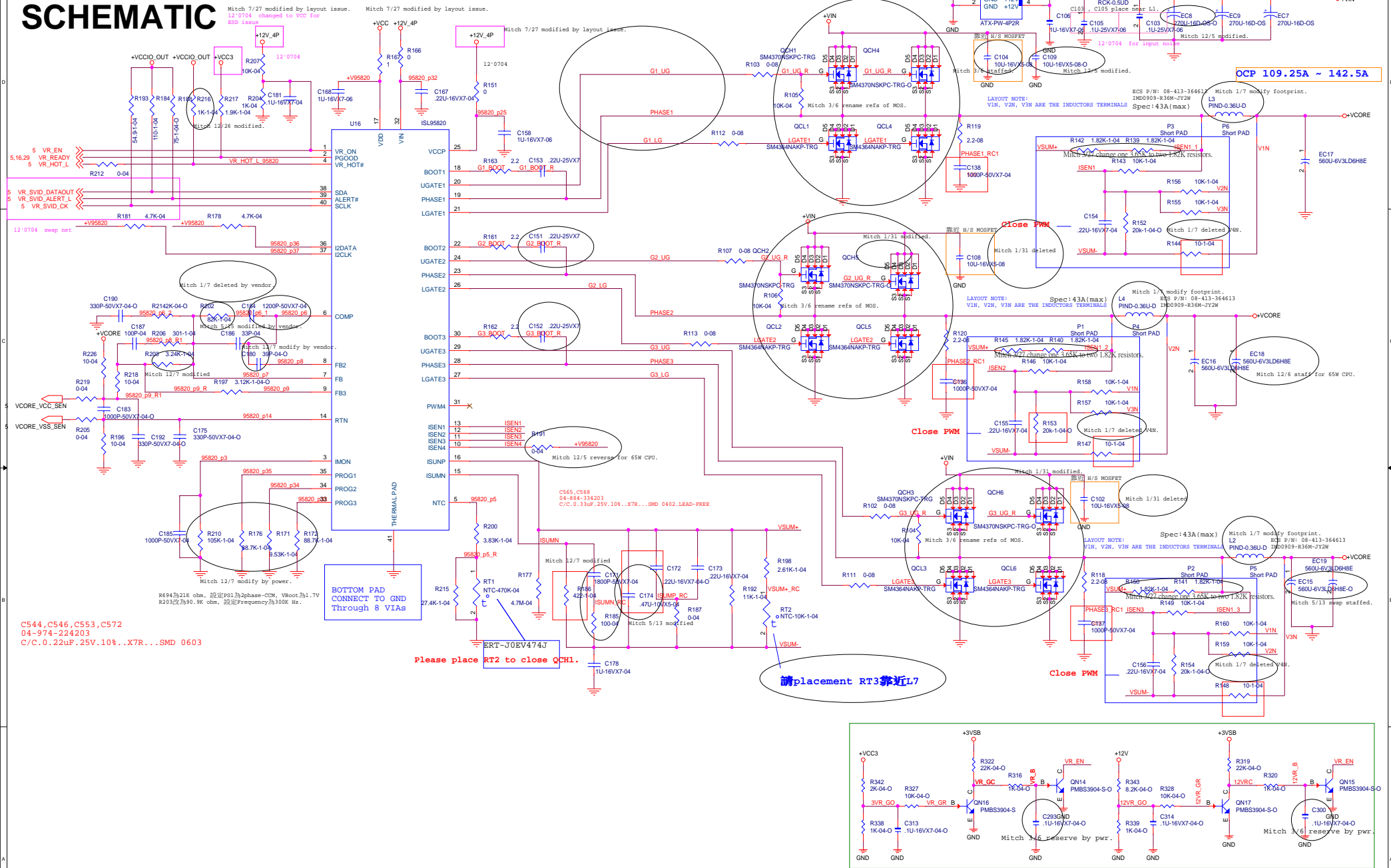
SPI ROM & PCH Power Circuit



+VCC3_EPW	Ld	Le	Lf
Intel LAN	X	V	X
Realtek LAN	V	X	X
Intel LAN(Cost down)	X	X	V



ISL95820 FOR VR12.5 RFQ SCHEMATIC



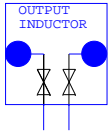
VRM Sequencing Circuit

Title			
VR12.5 SOLUTION ISL95818 SUGGEST SCHEMATIC			
Size C	Document Number H81H3-AD	Rev 1.0	
Date:	Friday, June 07, 2013	Sheet	33 of 37



Mitch 3/21 deleted for multi rail PSU.

SPxx PLACE ON THE
SOLDER SIDE,
CLOSE INDUCTOR



The Rs1, Rs2 and C can be calculated as:

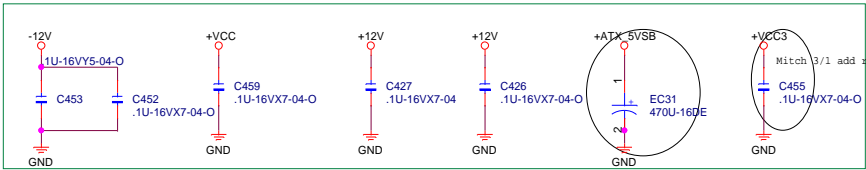
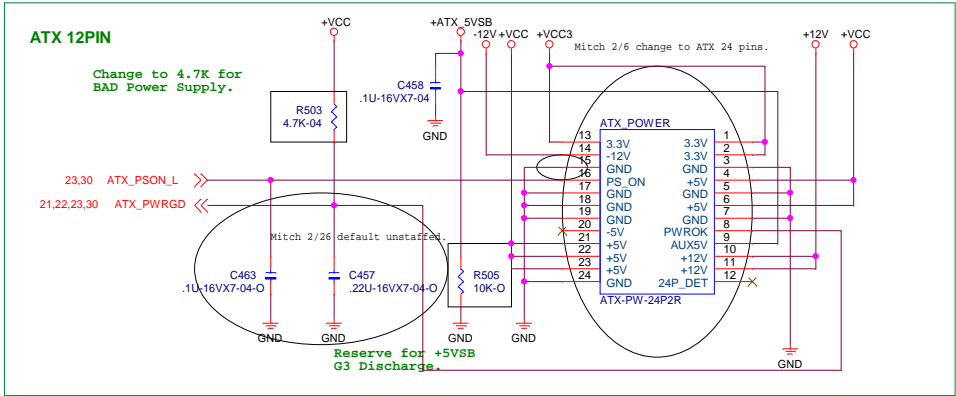
$$C \cdot (R_{S1} // R_{S2}) = \frac{L}{DCR}$$

The inductor peak current limit is:

$$I_{LIM(Peak)} = \frac{V_{th,DC}}{k \cdot DCR}, \text{ where } k = \frac{R_{S2}}{R_{S1} + R_{S2}}$$

The DC current limit is:

$$I_{LIM} = I_{LIM(Peak)} - \frac{V_O \cdot (V_{in} - V_O)}{2 \cdot V_{in} \cdot f_{SW} \cdot L}$$



Mitch 5/20 staff for drop issue on S5 to S0.

Title DC/DC VDIMM/DDR_VTT1/SVDUAL		
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